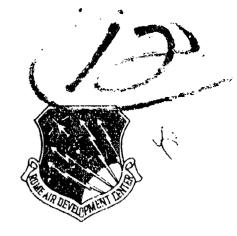
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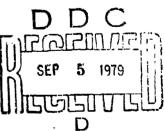
RELIABILITY TEST AND EVALUATION OF MIL-M-38510 LINEAR MICROCIRCUITS

McDonnell Douglas Astronautics Company

Roy C. Maurer

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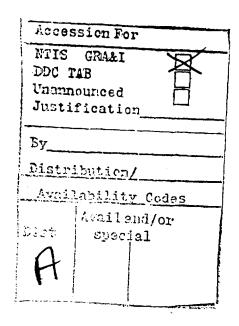
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PREFACE

The work described in this report was performed by the Parts Evaluation Laboratory section of the McDonnell Douglas Astronautics Company-St. Louis Engineering Reliability department during the period between July 1976 and November 1978. The work was performed for the USAF Rome Air Development Center under Contract Number F30602-76-C-0371. The RADC project engineer was W. Keith Conroy. Significant technical contributions were made by Messrs. Gordon Johnson, Gary Keller, Ron Mackin, Michael Roberts and Edward Sisul.



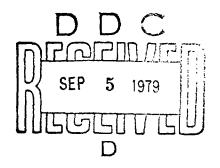


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EVALUATION

It is usually desirable, but not always possible, to fully characterize and evaluate the reliability of linear microcircuits before a MIL-M-3851C detail specification is generated. The specification must be verified to prevent manufacturers from qualifying inferior products either because the specification doesn't accurately reflect the screening conditions that were intended, or these conditions, however accurate, are insufficient. In this effort, both the selected linear devices and their respective detail slash sheems were evaluated. After the specifications were verified, sample parts were screened to the verified specification, stressed, and tested in order to measure their fitness for military applications. The result of this screening and testing is a reliability determination based on a failure rate extrapolation. The reliability data generated in this contractual effort will be used to determine which vendors of the products tested have potential for supplying reliable, military grade linear microcircuits, and also to provide some insight into the state of the art in linear microcircuit production. In addition, the vendors participating in this study can use the failure analysis data provided to amprove their product which will result in increased yield, higher reliability, and lower cost. Recommendations for improvement of the procurement specification will be implemented in both MIL-STD-883, "Test Methods and Procedures for Microelectronics," and MIL-M-38510, "General Specification for Microcircuits," resulting in an improved standard for procuring reliabile linear microcircuits as part of the R5R TPO thrust in Solid State Device Reliability.

N. Keich Conroyf. W. KEITH CONROY, JR.

Project Engineer

1.0 INTRODUCTION

The objective of this program was to evaluate the reliability of selected MIL-M-38510 linear microcircuits. Included in the evaluation were a) device electrical characterizations, b) analyses of device physical characteristics, c) determinations of device thermal characteristics, and d) high temperature accelerated test studies of device aging characteristics. Results of the evaluation were intended to provide information related to the following:

- a) Adequacy of MIL-M-38510 specifications and test methods of the selected linear devices.
- b) Relationship of device physical characteristics and processing techniques to device reliability,
- c) Failure mechanisms.
- d) Failure distributions at accelerated test conditions, and
- e) Arrhenius model parameters and failure rates.

This report provides a general description of the overall program and presents the results of tests and evaluations performed prior to, during, and subsequent to long-term high temperature accelerated life tests. Included in these tests are all tests and evaluations required as a prerequisite to initiating long-term high temperature life testing, as well as the interim and final electrical measurements, results of characterization testing, analysis of failed devices, and analysis of failure data to determine device aging characteristics.

2.0 PROGRAM DESCRIPTION

The overall reliability test and evaluation of the MIL-M-38510 linear microcircuits program is depicted in Figure 1. A total of five device types from two manufacturers each were included in the program. The specific device types and manufacturers are shown in Table 1. At the time of procurement both the LM109 and the 78M05 devices were specified in MIL-M-38510/10701 as electrically equivalent 5 volt regulators, and the LM109 was only available from Manufacturer B. Therefore, the Manufacturer D 78M05 was used as the second source for the LM109 regulator. However, for clarity, the Manufacturer D device is referenced as a LM109 throughout this report. A total of 150 of each manufacturer's device type were procured to MIL-M-38510 Class B, or equivalent processing requirements. Upon receipt at MDAC-St. Louis, all devices were subjected to external visual examination, hemseticity tests and electrical tests. The electrical testing consisted of MIL-M-38510 Group A. dc tests at 25°C, -55°C and 125°C. However, when a high percentage of devices failed to meet the MIL-M-38510 parameter limits, the end-point limits were adjusted as required, to obtain an adequate number of devices for accelerated life testing.

Subsequent to performing the initial examinations and tests, acceptable devices were assigned by serial number to test groups. Device allocation for each manufacturer's device type is shown in Figure 1.

Electrical characterization testing was performed to provide a complete description of the electrical characteristics of each manufacturer's device type. The testing included, in addition to the initial dc electrical tests performed with all devices, sample tests of ac parameters and transfer characteristics.

Construction analyses require destructive physical analyses to determine construction methods, manufacturing process techniques and workmanship used in the fabrication of devices. Results were used to predict potential reliability problems, determine possible accelerated life test limitations (due to materials used in device fabrication), and to facilitate subsequent failure analyses.

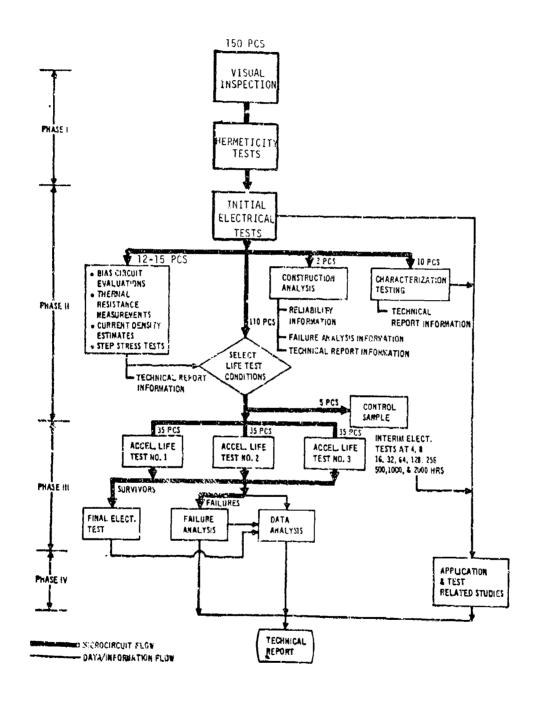


FIGURE 1. LINEAR MICROCIRCUIT TEST PROGRAM

TABLE 1. LINEAR MICROCIRCUIT TYPES

M38510 PART NO. REFERENCE	COMMERCIAL PART NO.	PART TYPE	MFR	PROCUREMENT SPEC
M38510/10104 BGC	LM108A	OPERATIONAL AMPLIFIER	A B	MFR'S ELECTRICAL* MFR'S ELECTRICAL*
M38510/10107 BGC	LM118	OPERATIONAL AMPLIFIER, HIGH SPEED	C B	MFR'S ELECTRICAL* MRF'S ELECTRICAL*
M38510/10201 BIC	723	PRECISION VOLTAGE REGULATOR	D C	JM38510 MFR'S ELECTRICAL*
M38510/10304 BGC	LMIII	PRECISION VOLTAGE COMPARATOR/BUFFER	D B	MFR'S ELECTRICAL* MFR'S ELECTRICAL*
M38510/10701 BXC	78M05 LM109	VOLTAGE REGULATOR, 5 VOLT	D B	MFR'S ELECTRICAL*

^{*} DEVICES WERE TO MEET THE MIL-M-38510 ELECTRICAL CHARACTERISTICS, BUT DID NOT NEED TO BE TESTED TO THESE REQUIREMENTS IF JAN TEST TAPES WERE NOT AVAILABLE.

The initial device studies were prerequisite to performing the accelerated life tests and included an evaluation of the MIL-M-38510 bias circuits for accelerated testing, development of new bias circuits as required, and thermal resistance measurements for computing device junction temperatures at anticipated test temperatures.

Three accelerated life tests were performed to provide information about device failure mechanisms, failure distributions and life acceleration factors. Actual life test temperatures were determined from results obtained in bias circuit evaluations and step-stress tests. Each life test was conducted for 4,000 hours or a minimum of 50% failure, whichever occurred first. Interim electrical tests were performed on life test devices after cool-down to room temperature with bias applied. These measurements consisted of MIL-M-38510 dc tests at 25°C and were performed at 4, 8, 16, 32, 64, 128, 256, 500, 1,000 and 2,000 hours of life testing. Unless otherwise directed by the Project Test Engineer, all parts that failed an interim test were removed from the life test and subjected to failure analysis. At the conclusion of each life test, surviving devices were subjected to the same set of MIL-M-38510 electrical tests performed prior to life testing.

A control sample of each manufacturer's devices was subjected to electrical testing each time the test devices were subjected to interim or final electrical tests. The purpose of the control sample was to provide a check on the long term stability of the automated test equipment.

Application and test related studies were performed to determine application-related reliability problems associated with system use of the linear devices included in this program. Application and test related experience derived throughout the program was used to develop design guides for items such as board layout, compensation, bypassing, and interfacing.

3.0 RESULTS OF PRE-LIFE TESTS AND EVALUATIONS

3.1 EXTERNAL VISUAL EXAMINATIONS AND HERMETICITY TESTS

Upon receipt at MDAC-St. Louis, all devices were examined for conformance to purchase order requirements for device type, package style, lead finish, and marking. Each device was examined at 3X magnification for evidences of gross damage to package, package seals, and leads. Fine and gross leak tests were then performed per MIL-STD-883, Method 1014.1, Conditions A1 and C2.

With one exception, no major visual or hermetic defects were found in the delivered devices. One manufacturer's devices were rejected for incorrect lead finish and were subsequently replaced. Results of examinations and tests performed with this manufacturer's replacement devices and all other manufacturers' devices are shown in Table 2.

Replacements for electrical test rejects were also subjected to visual examinations and hermeticity tests. Thus, the total quantity of devices shown in Table 2 exceeds, in some cases, the procurement quantity of 150 devices.

3.2 BASELINE ELECTRICAL PERFORMANCE TESTS

With the exception of the devices noted in Table 2, all devices surviving the initial visual inspections and hermeticity tests were subjected to electrical performance tests at 25°C, -55°C, and 125°C. These tests consisted of selected subgroups of the MIL-M-38510 Group A tests. Specific subgroups for the MIL-M-38510/10104 (LM108A), /10107 (LM118) devices were Al through A6. Specific subgroups for the MIL-M-38510/10201 (723) and /10701 (LM109) devices were A1, A2, and A3. The specific subgroups for the /10304 (LM111) device were A1, A2, A4, and A5. LM111 testing at -55°C (Subgroups A3 and A6) was not performed due to device/test fixture oscillation at -55°C. Details of the electrical test conditions and end-point limits used for testing each device type are contained in Appendix B. In most cases the end-point limits are those contained in the current MIL-M-38510 slash sheet. However, in several instances the end-point limits were relaxed to obtain a sufficient number of "good" devices for subsequent testing. A summary of the MIL-M-38510 parameter

TABLE 2. INITIAL INSPECTION AND HERMETICITY TEST RESULTS

(VISUAL 1	NSPECTION		HERMETIC	TY TESTS		TOTAL	SUBMITTED
				FINE	L(.V.	GR 05 5	LEAK	NO.	FCR
COMMERCIAL PART NO.	MANUFACTURER	NO. TESTED	NO. FAILED	NO. TESTED	NO. FAILED	NO. TESTED	NO. FAILED	FAILED DEVICES	ELECTRICAL TEST
LM108A	A	198	0	198	1	197	3	4	194
	B	150	2	148	1	147	3	6	144
LM118	С	150	0	150	D	150	3	3	147
	В	150	0	150	3	147	0	3	147
723	S	150	2	148	1	147	0	3	147
	Ç	188	3	185	0	185	0	3	185
LM111	D	150	0	150	2	148	0	2	129 1 25
	В	150	0	150	0	150	0	0	133 🛆 🕰
7805	D	150	1	149	1	148	u	ż	145
LM109	В	150	0	150	0	150	1	1	149

 ^{△ 3} Devices used for construction analysis and 3 devices were subjected to Gas Mass Spectrometer Analysis.
 △ 13 Devices used for test fixture development.
 △ 11 Devices used for test fixture development.

limits that were revised is shown in Table 3. Results of the initial electrical testing using the revised end-point limits are summarized in Table 4. Parametric data taken at 25°C is shown for each device type in Tables 5 thorugh 9. The tables providing parametric data contain the parameter limits, a computed mean value of the parameter for all devices meeting the revised specification limits, and a computed standard deviation of the measured parameter values. Examination of the test data revealed no marked differences between manufacturers for the majority of parameters. However, the gain tests on both the LM108A and LM118 devices do show a difference of approximately one order of magnitude. This is caused by nonlinearities in the dc transfer responses and is discussed in more detail in Appendix E. Also the ${
m I}_{10}$ values for the LM118 devices differ by an order of magnitude. The LM109 also exhibited an appreciable difference in line regulation ($V_{\rm PLN}$) and load regulation (V_{RLD}) parameters. Manufacturer D's devices exhibited better line regulation while Manufacturer B's devices exhibited better load regulation. The Manufacturer D device was actually a 78M05 device, and has different circuit design which accounts for the differences in these characteristics.

The only JAN qualified device was Manufacturer D's MlL-M-38510/10201 of which five devices were rejected. There were two visual, one hermetic, and two electrical failures noted in the initial examination of the JAN devices. All data on the failed devices can be found in Appendix G.

3.3 MICROCIRCUIT CONSTRUCTION DETAILS

A destructive physical analysis of at least two of each manufacturer's device type was performed to determine the materials, construction methods, process techniques and quality of workmanship used in the device fabrication. Complete results of these analyses including schematics and chip topography are contained in Appendix A. With the exception of the basic package type and material, no major construction differences were noted between manufacturers' device types. All devices had the following construction characteristics in common, a) aluminum internal wire and chip metalization, b) gold plated Kovar external lead and internal post, c) gold-silicon die attach, and d) a welded

TABLE 3. REVISED MIL-M-38510 PARAMETER LIMITS

M71.44.38510	SUBGROUP	PAGAMETER	#11# []	FIL-M-38510 LIXIT		REVISED LIMIT	STITS	M114-38510		PARAMETER (TES) W.)	h11-4-38510 LIMIT	01288 17	SEVISSO	8.	
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	,	START			₁		-								

YABLE 4. INITIAL ELECTRICAL TEST RESULTS

DADE		NO INTO			AVAILABLE		
PART NO.	MFR	NO. INTO TEST	25°€	125°C	- 55°C	TOTAL	FOR TEST
723	D	147	6	4	4,	6 🛕	141
723	C	185	40	9	39	62	1.23
LM108A	В	• 144	4	17	9	27	117
LM108A	A	194 🐴	42	13	10	51	143
LM118	C	147	2	11	0	13	134
LM118	В	147	4	6	5	13	134
LM109	В	149	5	4	6	13	136
M109	D	148	0	10	136 🖄	10	138
LNS 11	В	133	4	4	<u> (3</u>)	4	129
LM11!	D	129	4	3		4	125



Four (4) parts were destroyed by test equipment failure.



Two (a) parts also failed at 125°C. The remaining 134 were -55°C V_{START} parameter test failures which were ignored for the life test program.



⚠ The -55°C tests were pot performed for this device due to excessive oscillation.



4 Of the 194 devices which were submitted for electrical tests, 28 devices failed the initial 25°C electrical tests and were returned to the manufacturer for replacements. Since the 125°C and -55°C electrical tests were not performed on the 28 returned devices only 166 devices were tested at -55°C and 125°C.

TABLE 5. M38510/10104 (LM108A) INITIAL FLECTRICAL 25°C PARAMETER CHARACTERIZATION

	_			MANUFACT	URER B	MANUFACT	TURER A	
PARAMETER	TEST	LIMI	TS	MEAN	SIGMA	MEAN	SIGMA	UNITS
	NOS.	MIN	MAX					
v _{IO}	1-4	-0.5	+0.5	-0.007	0.204	-0.003	0.137	mV
+A _{VS}	71	80		1,614	1,892	865.8	1,568	V/mV
-A _{VS}	72	80	~	1,920	3,039	203.5	87.26	V/mV
+A _{VS}	75	20		1,120	1,373	252.6	255.2	V/mV
-A _{VS}	76	20		2,934	8,859	141.4	47.95	V/mV
u _I	5-8	-0.2	+0.2	-0.012	0.041	-0.007	0.026	nA
IB	9-12	-0.1	2.0	1.067	0.413	1.056	0.305	nΑ
-I _{I8}	13-15	-0.1	2.0	1.078	0.415	1.063	0.302	nA
+PSRR	17	0	16	0.470	1.636	2.438	0.903	μV/V
-PSRR	18	0	16	1.707	0.925	1.118	2.078	μV/V
CMR	19	96		124.7	8.916	121.124	7.240	dB
+I _{OS}	22	-15	-2.0	-5.406	0.155	-9.033	0.627	mA
-1 _{0S}	23	2	20	11.41	0.269	12.289	4.302	mA
P _Ū	24	2	24	11.38	0.874	13.958	2.584	Wm
v _{OP+}	67	16		13.493	0.090	19.167	0.078	Vp
V _{OP} -	68		-16	18.836	0.056	18.914	0.064	\v_p

TABLE 6. M38510/10107 (LM118) INITIAL ELECTRICAL 25°C PARAMETER CHARACTURIZATION

					URER C	MANUFAC	TURER B	
PARAMETER	TEST NOS.	LIMI MIN	TS MAX	MEAN	SIGMA	MEAN	SIGMA	UNITS
v ₁₀	1-4	-4.0	+4.0	0.053	1.273	-0.319	1 393	mV
+A _{VS}	69	80		2068	3915	151.9	29.11	Y/mV
-A _{VS}	70	80		2966	8711	112.0	16.46	V/mV
+A _{VS}	71	80		964.4	2321	154.0	81.50	V/mV
-A _{VS}	72	80		140.9	129.9	174.9	65.18	V/mV
^{+A} vs	73	40		161.2	129.1	169.5	98.31	V/mV
-A _{VS}	74	40		228.9	778.1	115.9	18.21	V/mV
+A _{VS}	75	40		525.8	1037	123.2	70.73	V/mV
-A _{VS}	76	40		738.6	1852	1139.8	3037	V/mV
IIO	5-8	-40	+40	-9.499	9.523	-0.317	6.401	nΑ
+I _{IB}	9-12	+1	250	173.5	31.44	168.0	23.82	nA
-I _{IB}	13-16	. +1	250	187.0	31.23	111.2	24.05	nA
+PSRR	17	0	100	-14.768	10.15	-26.08	10.37	μ ۷/۷
-PSRR	18	O	100	-35.373	12.13	-14.95	6.447	μV/V
CMR	19	80		100.1	6.568	105.3	8.658	₫B
V _{IO ADJ(+)}	20	7.5		16.92	1.193	12.52	0.830	mV
V _{IO ADJ(-)}	21	7.5		-16.83	1.397	-12.68	0.844	mV
I ₀₅ (+)	22	-40	-12	-30.19	1.358	-31.18	1.205	mA
I ₀₅ (-)	23	12	55	24.94	2.533	39.42	1.553	mΑ
PD	24	10	280	204.3	11.65	262.6	9.72	mW
V _{OPP}	57	34		37.81	0.147	37.77	0.117	٧ _{p-} p
V _{OPP}	6 8	32		3ი, 60	0.138	36.25	0.123	V _{F=P}

	· · · · · · · · · · · · · · · · · · ·			MANUFAC	TURER D	MANUFAC	MANUFACTURER C		
PARAMETER	TEST	LIMITS		MEAN	SIGMA	MEAN	CICNA		
· · · · · · · · · · · · · · · · · · ·	NO.	MIN	мах	CIEMN	310MA	MEAN	SIGMA	UNITS	
V _{RLINE}	1	-0.10	0.10	-0.017	0.004	-0.019	0.011	% V _{OUT}	
V _{RLINE}	2	-0.3	0.3	-0.117	0.029	-0.141	0.049	% V _{OUT}	
V _{RL INE}	3	-3.2	0.2	-0.011	0.005	-0.013	0.010	% V _{GUT}	
V _{RLOAD}	4	-0.15	0.15	-0.011	0.009	-0.007	0.010	% V _{OUT}	
V _{RLOAD}	5	-0.5	0.5	0.000	0.014	0.001	0.005	[≈] v _{out}	
V _{RLOAD}	6	-0.2	0.2	0.003	0.008	0.003	0.003	≈ v _{out}	
VREF	7	6.95	7.35	7.243	0.056	7.208	0.097	٧	
ISCD	8	0.5	3.0	2.472	0.143	2.185	0.412	mA	
I _{0S}	9	45	85	59.19	5.217	58.58	2.801	πι A	

TABLE 8. M38510/10701 (LM109) INITIAL ELECTRICAL 25°C PARAMETER CHARACTERIZATION

				MANUFACT	URER D	MANUFAC			
PARAMETER	TEST			MEAN	SIGMA	MEAN	SIGMA	UNITS	
PARAMETER	NO.	MIN	MAX	PILAN	310/IA	TILAN	STUMA	UNITS	
ν _{CUT}	1	4.80	5.20	5.039	C.061	5.044	0.042	Vdc	
V _{OUT}	2	4.80	5.20	5.003	0.060	5.044	0.641	Vdc	
V _{OUT}	4	4.80	5.20	5.031	9.063	5.029	0.044	Vdc	
V _{RLN}	6	~20	+20	5.710	2.626	-17.388	1.908	mVdc	
V _{RLD}	7	-50	+50	35.689	3.510	-2.798	2.626	m∀dc	
I _{SCD}	9	-10.0	0	-4.084	0.350	-7.168	0.342	m.Adc	
Isco	10	-10.0	0	-4.070	0.367	-7.224	0.367	mAdc	
^I scD	וו	-10.0	0	-4.056	0.349	-7.130	0.368	mAdc	
ΔI _{SCD}	12	-0.8	-0.8	0.014	0.047	-0.056	0.046	mAdc	
ΔI _{SCD}	13	-0.5	0	-0.028	0.028	-0.038	0.067	mAdc	
Ios	14	-2.0	-0.7	-0.905	0.149	-1.221	0.003	Adc	
V _{START}	15		9 0	5.017	0.061	5.037	0.046	Vdc	

TABLE 9. M38510/10304 (LM111) INITIAL ELECTRICAL 25°C PARAMETER CHARACTERIZATION

		<u> </u>		MANUFAC	TURER D	MANUFACTURER B		
PARAMETER	TEST	LIM	ITS	MEAN	SIGMA	MEAN	SIGMA	UNITS
PARAPLICA	NOS.	MIN	MAX	TIEAN	310///	III AII	STUMA	01417.3
v ₁₀	1-4	-4	+4	335	.414	243	.458	mV
۷ _{10(R)}	5-7	-4	+4	743	. 3 89	229	.467	m۷
AVC+	92	150	-	459	73.3	925	1354	V,′ _{mV}
AVC -	94	150	-	302	88. 8	1371	2028	V/ _{mV}
10	8-10	-10	+10	-678	1.66	1.24	1.18	nA
^I 10(R)	11	-25	+25	3.99	4.44	3.81	3.15	nA
I _{IB+}	12-14	150	+.1	-56.4	27.4	-53.8	14.7	nA
I _{IB} -	12-14	-150	+.1	-57.1	27.8	-55.0	15.0	nA
V _{IO(ADJ)+}	23	4	-	8.829	.289	5.22	.251	mV
V _{IO(ADJ)} .	24	_	4	-8.81	.290	-5-369	.266	m¥
CMRR	25	75	-	105	5.76	110	5.95	dB
V _{OL 1}	26-27	0	.400	.230	.018	.276	.015	٧
V _{OL 2}	28-29	0	1.500	.833	.021	.915	.037	٧
¹o	16	0	.500	.123	.007	.123	.007	μА
^I G	17	-10	0	855	.96 6	-1.30	1.34	μА
III	18	0	.100	.048	.003	.048	.003	μА
112	19	0	.100	.049	.003	.048	.004	μА
+I _{CC}	20	.5	5.0	4.11	. 244	3.25	.267	m A
-1 _{CC}	21	-4.0	5	-2.95	. 226	-2.306	.209	mA
105	22	70	200	164	5.01	140	13.0	mA
PĎ	15	30	270	211	13.9	167	14.1	m₩

lid seal. A summary of the differences in package type and material is shown in Table 10. There were no physical features observed that would have a major impact on life test results or would limit life test temperature to below 250°C.

Thirty devices (three of each manufacturer's device type) were subjected to Gas Mass Spectrometer Analysis. This analysis was performed by RADC and the results are shown in Table 11. Manfacturer D's 723 devices contained only traces of oxygen and carbon dioxide, but his LM111 devices contained significant amounts of water vapor, argon, and carbon dioxide. All of Manufacturer B's devices (LM108A, LM118, LM109, and LM111) contained only nitrogen and carbon dioxide, suggesting that this manufacturer has good control of the package atmosphere during device fabrication. Although surface related mechanisms are related to water vapor content in the package, the life test results disclosed not fiference between devices with or without water vapor.

3.4 BIAS CIRCUL: "LUATION

Short-term high temperature tests of a sample of each manufacturer's device type were conducted to a) verify the suitability of the MIL-M-38510 bias circuit for operating devices at ambient temperature up to 250°C, or b) evaluate candidate life test bias circuits for those device types that iid not operate satisfactorily in the MIL-M-38510 bias circuit. A suitable bias circuit was considered to be one that maintained maximum rated voltage across the device without causing excessive current at ambient temperature up to 250°C. A constant output voltage over the desired life test temperature range was also desired.

The bias circuit tests indicated that the LM108A, LM109, and LM111 devices were capable of operating at temperatures up to 250°C without exhibiting thermal runaway. Thermal runaway was encountered with the 723 and LM118 devices, at ambient temperatures above 200°C.

TABLE 10. MICROCIRCUIT CONSTRUCTION DIFFERENCES

PART TYPE	MANUFACTURER	PACKAGE TYPE	PACKAGE MATERIAL	
M38510/10104	В	T0 ~9 9	Nickel	
LM108A	A	T0-99	Au Plated Nickel	
M38510/10107	В	T0-99	Nickel	
LM118	С	T0~99	Ni Plated Kovar	
M38510/10201	С	10 Lead TO-5	Nickel	
723	D	10 Lead TO-5	Nickel	
M38510/10304	D	8 Lead T0-5	Nicke1	
LM111	В	8 Lead T0-5 ·	Nickel	
M38510/10701	В	T0-5	Nickel	
LM109	D	T0~5	Nickel	

TABLE 11. SUMMARY OF GAS MASS SPECTROMETER ANALYSIS

	·			COM	CENTRATION	¥ (V/V)				
CONSTITUENT	LM	108 A	LM	118	18 LH109		723		LM111	
	MSR A	MFR B	HER B	MFR C	MFR B	MFR D	MFR C	MFR D	MFR B	#.FR D
NI TROGEN	98.77	99.87	99.97	99.77	99.87	99.77	99.67	99.97	95.93	99.57
CARSON DIOXIDE	0.17	0.10	0.03	0.17	0.10	0.10	0.10		0.03	0.10
NUĐÂN	0.33					ļ 1				0.50
WATER VAPOR	0.53			0.03		0.13	0.23			0.17
OXYGEH	0.20			0.03						

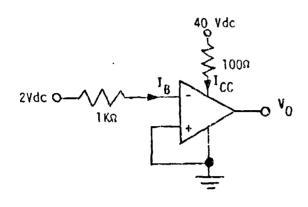
NOTE: YALUES ARE AVERAGES OF THREE DEVICES

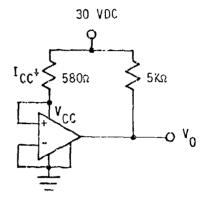
The bias circuits used for each accelerated life test are shown in Figure 2. The details and results of the bias circuit evaluation are contained in Appendix D.

3.5 STEP STRESS TESTS

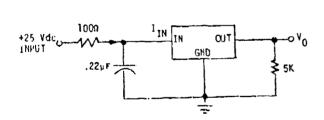
When a non MIL-M-38510 bias circuit was used, step stress testing was performed to evaluate that circuit and to obtain additional device failure data to aid in the final determination of accelerated life test conditions. Step stress testing was performed on the LM108A, LM118 and LM111 devices. Five of each manufacturer's devices were operated in the selected bias configuration for 16 hours in a test oven at 75°C. After 16 hours of operation at 75°C, devices were allowed to cool down under bias, and electrical testing was performed at 25°C. The surviving devices were then returned to test at an ambient temperature of 100°C for an additional 16 hours of operation. This sequence was repeated in 25°C increments until all surviving devices experienced thermal runaway at 275°C. Thermal runaway was not observed in the LM111 devices. The results of the LM108A, LM118, and LM111 step stress tests are shown in Table 12.

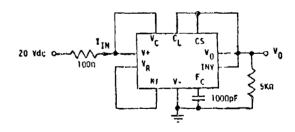
With the exception of the Manufacturer C LM118 devices, all LM108A and LM118 failures were due to bake recoverable surface related mechanisms. The Manufacturer C LM118 devices experienced a thermal runaway failure mode at 200°C and exhibited melted open metalization due to excessive current. Prior circuit evaluation tests had indicated a thermal runaway problem above 225°C. Thermal runaway was not observed with the Manufacturer B LM118's since all devices had failed after the 150°C step due to a surface related mechanism. As a result of these findings, LM118 life test temperatures were limited to a maximum of 175°C to avoid thermal runaway and to enhance the failure time resolution of Manufacturer B devices at the maximum test temperature.





MIL-M-38510/10104 (LM108A) MIL-M-38510/10107 (LM118) MIL-M-38510/10304 (LM111)





MIL-M-38510/10701 (LM109)

MIL-M-38510/10201 (723)

FIGURE 2. ACCELERATED LIFE TEST BIAS CIRCUITS

TABLE 12. STEP STRESS RESULTS

MANUF ACTURER	D/N	CUMULATIVE NO. OF FAILURES									NOTES
PARTO ACTORER	P/N	75°C	100°C	125°¢	150°C	175°C	200°C	225°C	250°C	275°C	MOTES
8	LM108A	0	o	1	2	3	3	4	4		2,4
_ A	LM108A	0	0	0	0_	0_	0_	0	0	l	2
В	LM118	0	0	3	5						4
c	LM118	0	0	0	0	0	1	1	2	4	3,5
В	LM111					3	3	3	3	5	6
D	LM111					0	1	2	2	3	7

- 1. Each test started with five (5) devices, and each temperature step lasted 16 hours.
- 2. Devices drew excessive current at 275°C. Step stress test terminated @ 250°C.
- 3. Devices drew excessive current at 275°C. Step stress terminated after 1/2 hour @ 275°C.
- 4: All failures were due to surface instability.
- 5. All failures were due to thermal runaway.
- 6. Two gevices failed $\mathbf{I}_{\mbox{IB}}$ due to operation of device near the saturation limit of the amplifier and three failed ${\bf I}_{10}$ due to surface instability. 7. One device failed ${\bf I}_{10}$ and two devices failed ${\bf V}_{10}$ due to surface instability.

As had been suggested by the prior circuit evaluation test results, the LM108A devices did not exhibit thermal runaway at 250°C indicating that the maximum life test temperature for the LM108A's could be as high as 250°C. However, subsequent attempts to initiate life tests at 250°C did reveal a thermal runaway problem with a high percentage of devices, and the maximum test temperature was reduced to 225°C.

With the exception of two Manufacturer B LM111 device I_{IB} failures at the 175°C step, and two Manufacturer D LM111 device V_{IO} failures at 275°C, all LM111 step stress failures were due to out-of-tolerance I_{IO} parameters. The apparent failed values of I_{IB} were attributed to device operation at common mode voltages too close to the supply voltage. Therefore the baseline electrical parameters were revised and performed at common mode voltages (V_{CM}) of OV, -13.5V, and 12.0V rather than the OV, -14.5V, and 13.0V specified in MIL-M-38510/10304. Both the I_{IO} and V_{IO} failures were due to surface instability, therefore life testing at 250°C was considered reasonable.

3.6 THERMAL RESISTANCE DETERMINATIONS

Upon completion of the bias circuit evaluation and step stress tests, the thermal resistance of each manufacturer's device type was determined to estimate maximum junction temperatures that would be experienced during life testing. An electrical test technique utilizing the forward voltage of a substrate diode as a temperature sensitive parameter was used to determine device junction temperatures. A MDAC-St. Louis thermal resistance tester was used to make the substrate diode forward voltage measurements. This tester operates the device in a power dissipating mode for 99.9% of the time and only briefly (1 millisecond every second) forward biases the substrate diode. Ambient temperatures and circuit configurations were consistent with expected accelerated life test conditions during the time junction temperature measurements were being performed. However, the actual power dissipation was somewhat less than the expected life test conditions. Thus, the thermal resistance values determined from those tests were used to compute junction temperatures at the power dissipation conditions expected during life testing.

The results of these tests are snown in Table 13. Thermal resistance values for each device type are similar for both manufacturers, and the variations between device types are inversely related to die size.

3.7 CURRENT DENSITY DETERMENATIONS

The current density in the V_{CC} stripes of each manufacturer's device type was determined from measurements of V_{CC} stripe dimensions during construction analyses and measurements of device currents during bias circuit evaluations. Results of these calculations are shown in Figures 3 and 4 for ambient temperatures up to 250°C. The maximum calculated current density at anticipated life test temperatures was less than 1 x 10⁴ A/cm². Therefore only minimal metal migration failures were anticipated in 4,000 hours of 250°C life testing at current densities below 1 x 10⁴ A/cm².

TABLE 13. MICROCIRCUIT THERMAL RESISTANCE

PART NUMBER	MANUF.	THERMAL RESISTANCE JUNCTION TO AMBIENT OJA - °C/WATT	
MIL-M-38510/10104	А	107.8	
(LM108A)	E	118.2	
MIL-M-38510/10107 (LM118)	Ĉ	67.0	
	В	1 ; 79.0	
MIL-M-38510/10201	c	65.7	
(723)	D	65.5	
MIL-M-38510/10701	В	60.0	
(LM109)	Ū	75.0	
MIL-M-38510/10304	В	199.9	
(L.M111)	D	218.6	

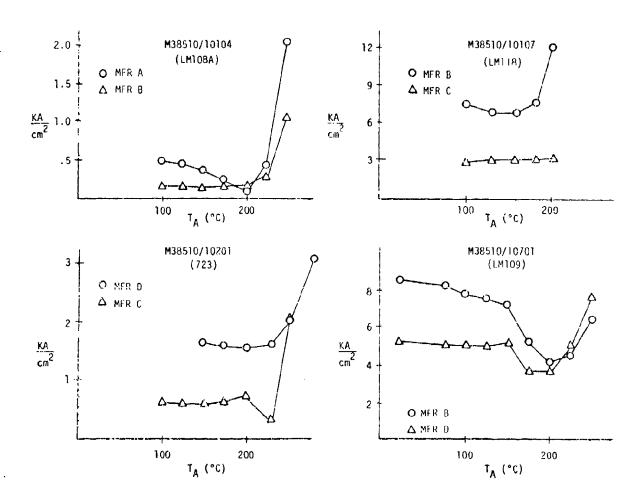


FIGURE 3. MICROCIRCUIT CURRENT DENSITY; LM108A, LM118, 723 & LM109

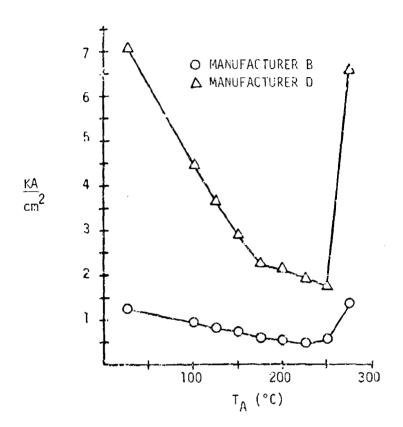


FIGURE 4. M38510/10304 (LM111) MICROCIRCUIT CURRENT DENSITY

4.0 ELECTRICAL CHARACTERIZATION TEST RESULTS

Characterization testing was performed in addition to initial baseline electrical tests to gain further insight into device performance characteristics. Those dynamic tests not performed during baseline testing such as rapple rejection, output noise, transient response, and slew rate, were performed with a sample of ten of each manufacturer's device type. The specific tests performed for each device are described in Appendix B. In addition, the transfer characteristics of two of each manufacturer's device type were evaluated at various conditions of temperature, voltage, Inad, and frequency. Summaries of the dynamic test results and details of the device transfer function studies are contained in Appendix E.

4.1 DYNAMIC TEST RESULTS

The dynamic test results are summarized in Table 14. At least 50% of each manufacturer's devices fail one or more of the dynamic parameter tests. Subsequent revisions to MIL-M-38510 contain relaxed end-point limits for these parameters. A review of the new specification limits and the data from these tests indicate that no further revisions of the specifications are necessary.

4.2 TRANSFER FUNCTION STUDIES

A study to determine the transfer function (the curve of the output response as a function of input voltage) of two of each manufacturer's devices was performed. The purpose of the study was to determine the response of transfer function curves to variations in temperature, voltage, load, and frequency.

The transfer function of the LM103A and LM118 operational amplifiers would ideally be the open-loop gain and would appear as in Figure 5. However, internal thermal effects cause the slope and linearity to change, as can be noted in Figures 6 and 7. In addition to Manufacturer B's LM108A and LM118 devices, the LM111 devices exhibited one or both of these thermal effects. Differences in phase and linearity are caused by thermal gradients which exist between the input and output circuits. These temperature gradients are produced by the

TABLE 14 DYNAMIC TEST RESULTS

	TOTAL FAILED									
DEVICE TYPE	MFR A	Mf R B	MFR C	MFR D						
LM108 A	7	10	-	-						
LM118	-	6	10	-						
723	-	-	10	5						
LM109	-	10	-	70						
LMIII	-	10 .	-	10						

¹ TEN (10) DEVICES OF EACH MANUFACTURER WERE SUBJECTED TO DYNAMIC TESTING.

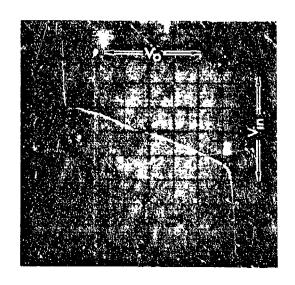


FIGURE 5. IDEAL OPERATIONAL AMPLIFIER OPEN LOOP GAIN CURVE

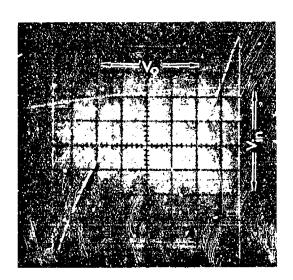


FIGURE 6. RESULTS OF THERMAL LITECTS ON THE IDEAL OPERATIONAL AMPLIFIER OPEN LOOP GAIN CURVE

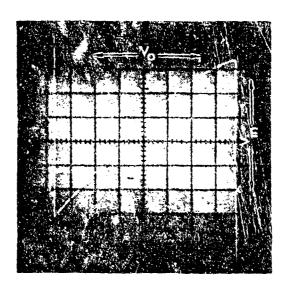


FIGURE 7. RESULTS OF THERMAL EFFECTS (180° PHASE SHIFT) ON THE MANUFACTURER B LM118 OPEN LOOP GAIN CURVE

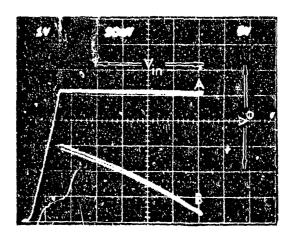


FIGURE 8. TYPICAL VOLTAGE REGULATOR TRANSFER CHARACTERISTIC CURVE

power dissipated in the output stages of the amplifier. The resulting heat conducts through the silicon chip causing uneven heating of the input components. Since all input components are not on isothermal lines, the resulting temperature differences in these components cause the device to produce other than ideal open loop gain curves.

The identification of device characteristics which produce linear transfer curves within operational amplifiers could not be fully determined. Although linearity is improved by minimizing temperature differences in the input circuitry, devices with nearly identical die layouts (Manufacturer B and C LM118) produce different transfer curves. Likewise, devices from different manufacturers with similar junction temperatures produced dissimilar transfer curves. In all cases the best transfer curves were obtained by operating the device at no load, thereby reducing the magnitude of the thermal effects within the die.

The transfer curve of the LM109 and 723 voltage regulators was normally a steady output voltage after there was sufficient input voltage to achieve turn-on. The curves in Figure 8 are typical of the voltage regulator transfer characteristic curve, and show the overall response (curve A), and a magnified response of the normal output of the device (curve B).

5.0 APPLICATION/TEST RELATED STUDY RESULTS

The application/test related studies were performed to provide information and recommendations related to the application of these linear devices in electronic equipment. Consideration was given to requirements for board layout, supply voltage filtering, shielding, compensation, loading, and interfacing. This information was derived from the results of characterization tests, development of electrical test programs and fixtures, and a literature survey of application guidelines. Test results were also used to formulate recommendations for improving the applicable MIL-M-38510 specifications.

5.1 APPLICATION GUIDELINES

The following recommendations are suggested as aids to optimal application of the linear devices studied in this program:

LM108A - The LM108A is a precision operational amplifier with very low offset voltage drift and high common mode rejection. The input is shunted with back-to-back diodes for evervoltage protection. Therefore the input differential voltage must be kept below 1 Vdc or excessive input currents will result. To improve power supply noise rejection, a 100 pF capacitor should be added from pin 8 to ground. In laying out a circuit using these devices care should be taken to keep package leads short and input leads close together, not only to minimize the possibility of parasitic oscillations and noise, but also to minimize offset errors due to thermal effects. Thermocouple effects, due to package lead to printed circuit board connections, can create microvolts of error if the temperature of the input lead connections differ by only a few degrees centigrade. Maintaining both ends of resistors at the same temperature is also important since carbon, oxide film and some metal film resistors can cause large thermocouple errors. Wirewound resistors of evenohim (20% Cr + 75% Ni + 2.75% Al + 2.75 Cu) or manganin (84% Cu + 12% Mn + 4% Ni) only generate about 2 µV/°C referenced to copper [1], but the inductance of wirewound resistors should be considered. Likewise, the gain fixing resistors should be of the same material to assure tracking with temperature. Since the device input bias currents are in the range of 1.0 nanoampere, care must be taken to reduce leakage currents by properly cleaning the printed circuit boards. To prevent subsequent contamination, the board should be covered with an epoxy or silicone rubber coating. To futher reduce leakage currents on a printed circuit board that has been properly cleaned and coated, a guard ring is suggested by both manufacturers. By designing the guard ring around the device input pins, as shown in Figure 9, the voltage differential between device pins is reduced, thereby reducing potential leakage currents.

LM118 - The LM118 device is a precision high speed operational amplifier with wide bandwidth and high slew rate. These devices also have diode input protection, but Manufacturer B's devices have a 1 volt breakdown limit while Manufacturer C's devices have a 5 volt breakdown limit. To achieve the high gain and large bandwidth of the device the circuit layout should be arranged to keep all lead lengths as short as possible and the output separated from the inputs. The values of the feedback and source impedance should be kept small to reduce the effect of stray capacitance at the inputs. The power supplies should be bypassed to ground at the supply leads of the amplifier with low inductance 0.1 $_{\rm L}$ capacitors. Capacitive loading must be kept to a minimum.

 $\underline{\text{LM109}}$ - The LM109 device is a complete five volt regulator. The regulator is current limited and goes into thermal shutdown at junction temperatures greater than 165°C. When operated at 25°C with no heat sinks, the device will go into thermal shutdown with a constant current load of 500 milliamperes. For a constant current of 500 milliamperes, proper heat sinks must be used. Output capacitors are not needed for stability, but a 1.0 $_{\rm LF}$ capacitor from the output to ground improves the transient response. Also, an input capacitor of 0.2 $_{\rm LF}$ is required if the regulator is located an appreciable distance from the power supply filter.

723 - The 723 device is a precision voltage regulator. The device has low standby current drain, low temperature drift, and high ripple rejection. The device can be used as a series, shunt, switching, or floating regulator in positive or negative power supplies. In using the device as a low voltage regulator the circuit shown in Figure 10 is used. For this circuit R3 should be equal to R1 in parallel with R2 for minimum temperature drift, since the device is susceptible to temperature drift under high dissipation conditions.

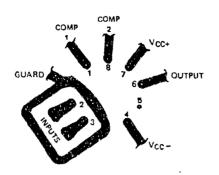


FIGURE 9. SUGGESTED PRINTED CIRCUIT BOARD LAYOUT OF INPUT PROTECTION FOR LM108

DEVICES

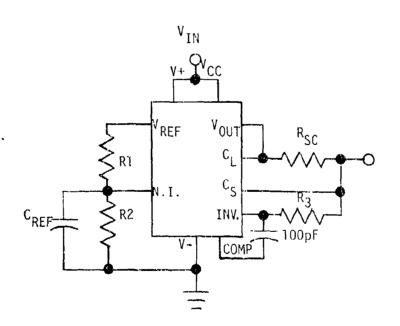


FIGURE 10. 723 APPLICATIONS CIRCUIT

LM111 - The LM111 device is a voltage comparator with input bias currents typically in the 50 nanoampere range. When the LM111 device is used in a circuit which does not use feedback, there are no special precautions to recommend, but in a feedback loop type circuit the device is susceptible to oscillations. To eliminate these oscillations lead lengths should be kept as short as possible and power supply bypass capacitors should be placed as close to the device as possible. Details of the compensation necessary to reduce oscillation for the MIL-M-38510 test circuit are contained in the next section.

5.2 STATIC TEST CIRCUIT MODIFICATIONS

The circuits used in the static electrical tests were those contained in the appropriate MIL-M-38510 specification. The compensation and filtering capacitors were as shown in the specification except as noted below.

- (a) Capacitors connected to the device under test were placed as close to the device as possible.
- (b) MIL-M-38510/10104 and /10107 (LM108A and LM118) an additional 1 microfarad capacitor was added from +V_{CC} (pin 7) to -V_{CC} (pin 4). This was done to eliminate transients caused by relay switching between the specific tests.
- (c) MIL-M-38510/10304 (LM111) The LM111 device in the static test circuit was extremely susceptible to oscillation. By constructing the test fixture as compact as possible and attaching all capacitors associated with the device under test directly to the test socket, the oscillations were eliminated or reduced to an acceptable level, except for the emitter gain tests. The oscillation could not be reduced to an acceptable level for the emitter gain test so this test was deleted from the testing sequence. Additionally, the $I_{\hat{0}}$ and $I_{\hat{G}}$ test parameters were out of tolerance and test repeatability was poor due to ripple and transient currents in capacitors used to stabilize the test fixture. The automated system used to test these devices measures an instantaneous rather than an average current. Thus, it was necessary to fabricate a separate test fixture for measuring the $I_{\hat{0}}$ and $I_{\hat{G}}$ parameters. Since the compensating capacitors also permitted large current transients through the relay

contacts used for switching between tests, the fixture used for the $\mathbf{1}_0$ and \mathbf{I}_G measurements was also used for \mathbf{V}_{0L} , \mathbf{I}_{CC} and \mathbf{I}_I measurements. The two circuits and their compensation capacitors are shown in Figures 11 and 12.

5.3 MIL-M-38510 ELECTRICAL TEST DLITCHENCHLS

During the course of preparing software for automated tests of the linear microcircuits, a number of deficiencies were noted in the MIL-M-38510 slash sheets. A brief description of each discrepancy is as follows:

- (a) MIL-M-38510/10104 and MIL-M-38510/10107 The static test circuit (Figure 8) in the 15 September 1975 revision of the specification has a 50K ohm resistor in the minus input to ground path. This should be a 50 ohm resistance to match the impedance to the positive terminal. This discrepancy was corrected in Amendment 3, dated 22 February 1977. In addition, the Power Supply Rejection Ratio (PSRR) test limits should be double sided since it is possible to have a negative PSRR.
- (b) MIL-M-38510/10304 With the exceptions of the $I_{\rm OS}$ and $I_{\rm T}$ tests, all LM111 test conditions require the inputs (LM111 device pins 2 and 3) to be the same voltage. During preparations for electrical testing, a separate power supply was programmed for each input. While checking out the static test fixture it was noted that separate power supplies could not provide exactly the same voltage to the test socket, and millivolt differences in these voltages caused invalid test results. The difference in these supplies should be less than +10 microvolts. To insure that identical voltage conditions were present on each input, two additional relays were added to the /10304 static test circuit. The first of these relays shorts pins 2 and 3 together when the same voltage is required on each input, thus eliminating the error induced when using a second power supply. A second relay was added which provides ground on the device inputs when both of the additional relays are energized, thereby eliminating the need for either power supply on the device inputs during many tests. By installing

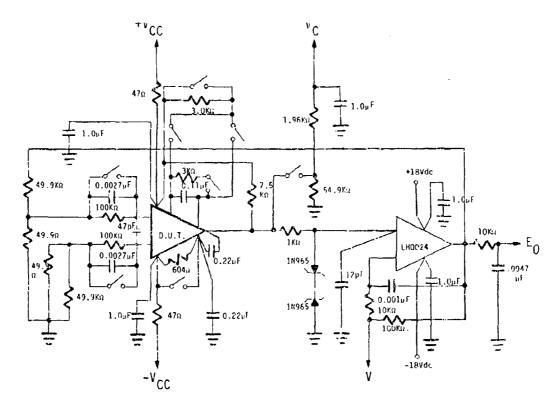


FIGURE 11. LM111 STATIC TEST CIRCUIT

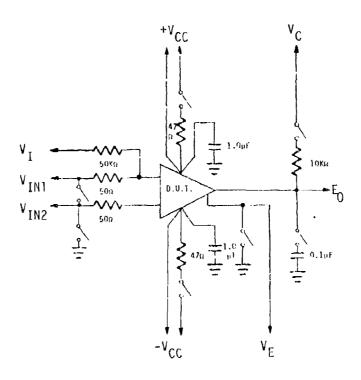


FIGURE 12. LM111 STATIC TEST CIRCUIT FOR I_0 , I_G , V_{0L} , I_{CC} AND I_I MEASUREMENTS

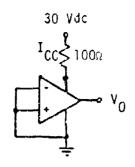
- the two (2) relays as close as possible to the test socket, invalid test conditions in the input offset voltages were eliminated. The static test circuit was also changed for the emitter gain test. The device under test should have $+V_{CC}$ connected to pin seven (?) to provide a voltage across the output transistor.
- (c, MIL-M-38510/10701 The test limits for the Delta Standby Current Drain (I_{SCD}) for the line current should be double sided since it is possible to have negative delta results.

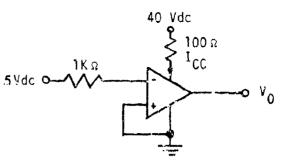
5.4 MIL-M-38510 ACCELERATED LIFE TEST CIRCUIT DEFICIENCIES

The circuits in MIL-M-38510/101D (15 September 1975), MIL-M-38510/101E (29 September 1977), and MIL-M-38510/103A did not provide adequate biasing conditions for accelerated life tests. New accelerated life test circuits were developed for the operational amplifier and the voltage comparator. The MIL-M-38510 bias circuits which were evaluated and the recommended life test bias configurations are shown in Figure 13.

The MIL-M-38510/1010 bias circuit, which applied 30Vdc to V_{CC} and ground to the device inputs, did not provide maximum stress conditions across the device. The MIL-M-38510/101E bias circuit increased the applied V_{CC} voltage from 30Vdc to 40Vdc which provided the maximum rated V_{CC} voltage across the device. However, by applying 5Vdc to the (+) input of the device this configuration allowed the input protection network to draw excessive current. The recommended bias circuit was preferred since it reduces the input current by lowering the input bias voltage from 5Vdc to 2Vdc in addition to applying the maximum rated device voltage (40 Vdc) across the devices.

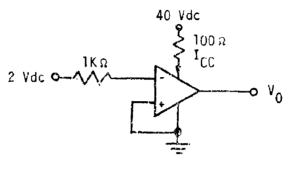
In the recommended life test bias circuit for the comparators, a 5K ohm current limiting resistor is connected between the output (pin 7) and the 30 Vdc power supply. The MIL-M-38510/10304 life test circuit has the output connected directly to $\pm V_{CC}$ (pin 8). In the MIL-M-38510/10304 configuration the voltage across the device would depend on the state of the device output, and if the cutput switched low there would be no voltage across the device. Any test circuit which does not insure that 85% of the supply voltage would



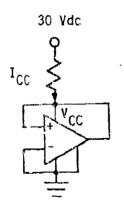


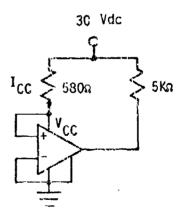
MIL-M-38510/101D AMPLIFIER LIFE TEST CIRCUIT

MIL-M-38510/101E AMPLIFIER LIFE TEST CIRCUIT



RECOMMENDED AMPLIFIER LIFE TEST CIRCUIT





MIL-M-38510/103A COMPARATOR LIFE TEST CIRCUIT

RECOMMENDED COMPARATOR LIFE TEST CIRCUIT

FIGURE 13. MIL-H-38510 VS. RECOMMENDED LIFE TEST CIRCUITS

always be present across the device is considered unacceptable. This condition was eliminated by connecting the device output to the power supply through a 5K ohm resistor.

Both recommended life test circuits provide adequate life test conditions and no bias circuit related failures resulted during the actual life tests.

5.5 MIL-STD-883 DEFICIENCIES

The MIL-M-38510/101E and MIL-M-38510/103B contain a Group A inspection table (Table III) which lists the electrical test requirements for the applicable linear devices. Within each table is a column of MIL-STD-883 test methods which can be referenced for most electrical tests. The information found in each referenced MIL-STD-883 test method can be categorized by one of the following:

- (a) The test method does not apply to the MIL-M-38510 electrical test in question.
- (b) The test method was written for testing of digital microcircuits, or
- (c) The test method is outdated by test information contained in the respective MIL-M-38510 slash sheet.

Since all Group A electrical tests for the LM108A, LM118, and LM118 devices can be implemented with the information found in MIL-M-38510, the column of MIL-STD-883 3000 and 4000 series test methods should be deleted, or the test methods should be revised.

5.6 DEVICE OPERATION CHARACTERISTICS

The MIL-M-38510/10304 (LM111) device was found to exhibit erratic behavior in the extreme common mode voltage regions. Analysis of device operation in these regions showed that electrical tests performed at common mode voltages of -14.5 Vdc and +13 Vdc resulted in device operation at or close to the saturation limits of the input transistors. Figure 14 shows a typical plot of $I_{\rm IB}$ current versus common mode voltage. At common mode voltages of -14.5 and +13 Vdc the device is at or near the point where it is driven into saturation. Thus, the output of the nulling amplifier is also driven into saturation, resulting in a large out-of-tolerance value of $I_{\rm IB}$. It is suggested that the tests on these devices be modified to common mode voltages of -13.5 Vdc and +12 Vdc.

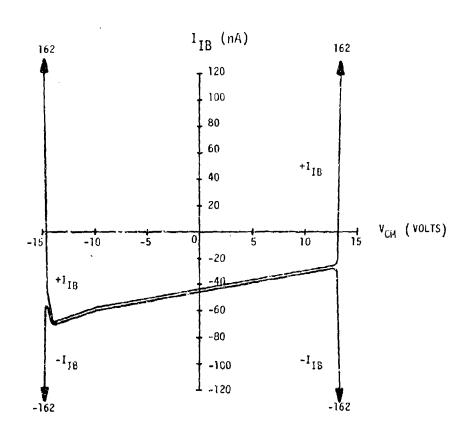


FIGURE 14 . PLOT OF M38510/10304 (LMIII) I $_{
m IB}$ VS. COMMON MODE VOLTAGE (V $_{
m CM}$)

6.0 ACCELERATED LIFE TESTS

6.1 LIFE TEST_CONDITIONS

Based on the results of the prelife test evaluations, the life test temperatures shown in Table 15 were selected. These temperatures appeared to avoid thermal runaway problems and the selected circuits maintained a constant device output voltage with minimal current drain. However, after operation of LM108A life test devices at 250°C for 1/2 hour, 43% of the Manufacturer A devices drew excessive current due to thermal runaway. The 15 devices which drew excessive current had a different date code (7642) than the devices used for circuit evaluation and step-stress (7643), and is apparently why this problem was not encountered during the prelife evaluations. Due to the thermal runaway problem, the maximum LM108A life test temperature was reduced to 225°C and the other two life tests were conducted at 200°C and 175°C. Unfortunately at 175°C, the output voltage of some of the Manufacturer B LM108As is low, whereas at 200°C and 225°C, the output of every device is thermally biased high. Although an undesirable condition, it was anticipated that most life test failures would not involve the output transistor, but would involve other transistors on the die where the junction stresses were the same at all temperatures. Actual failure modes for this device were not associated with the output transistors.

During initiation of LM111 life testing, more than 50% of the devices at life test temperatures of 225°C and 250°C failed within 32 hours. Almost all failures were due to slightly out-of-tolerance $\rm I_{10}$ and $\rm V_{10}$ values. In order to provide a reasonable failure distribution, the $\rm I_{10}$ and $\rm V_{10}$ limits were relaxed and life tests were continued. Previously failed devices were then subjected to the new failure criteria, and those passing were returned to life test. The $\rm I_{10}$ limits were changed from ±10nA to ±20nA and the $\rm V_{10}$ limits were changed from ±4mV to +5mV.

A summary of voltage, current, power dissipation, and junction temperature conditions at the selected ambient test temperatures is shown for each device type in Figures 15 through 19.

The sequence for performing the life tests is shown in Figure 20.

TABLE 15 LIFE TEST TEMPERATURES

		TEST	TLMPFRA	TURES (°C)	
PART TYPE	125	150	175	200	225	250
M38510/10104BGC (LM108A)			χ	Х	Х	x/ <u>1</u>
M38510/10107BGC (LM118)	Х	Х	Х			
M38510/10201BIC (723)		Х	X	χ		
M38510/10701BIC (LM109)				Х	X	Х
M38510/10304BGC (LM111)				Х	Х	Х
	<u> </u>			<u> </u>		

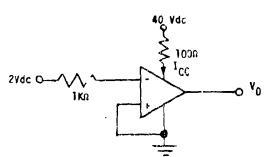
[/]l Initial attempts to operate LM108s at 250°C resulted in thermal runaway and the devices were subsequently placed on test at 175°C.

ACCELERATED LIFE TEST CIRCUIT

•		7	<u></u>	TOTAL CONTINUE OF THE			
	MANU- FACT- URER	TA AMBIENT TEMPERATURE (°C)	V _{CC} DEVICE VOLTAGE (VOLTS)	ICC DEVICE CURRENT (MICROAMPS)	Pd POWER DISSIPATION (MILLIWATTS)	V _O CUTPUT VOLTAGE (VOLTS)	TJ JUNCTION TEMPERATURE (°C)
	A	175	39.981	108	5.1	39.6	175.5
		200	39.994	61	3.3	39.6	200.4
		225	39.972	282	12.0	39.2	226.3
	8	175	39.988	173	7.8	15.6	175.9
		200	39.977	192	8.5	38.4	201.0
		225	39.961	340	14.4	34.6	226.7

- 1. DEVICE CONDITIONS ARE APPROXIMATE AVERAGE VALUES
- 2. JUNCTION TEMPERATURES BASED ON A CALCULATED THERMAL RESISTANCE (OJA) OF 107°C/WATT FOR MANUFACTURER A AND 118°C/WATT FOR MANUFACTURER B.

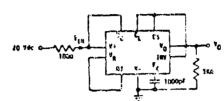
FIGURE 15. M38510/10104 (LM108A) SUMMARY OF LIFE TEST CONDITIONS



		A(CELERATED LIFE	TEST CIRCUIT		
MANU- FACT- URER	TA AMBIENT TEMPERATURE (°C)	VCC DEVICE VOLTAGE (VOLTS)	ICC DEVICE CURRENT (MILLIAMPS)	Pd POWER DISSIPATION (MILLIWATTS)	VO OUTPUT VOLTAGE (VOLTS)	T _J JUNCTION TEMPERATURE (°C)
С	125	39.70	3.0	119	1.44	132.9
	150	39.69	3.0	121	1.42	158.1
	175	39.68	3.0	122	1.58	183.2
8	125	39.78	1.9	76	.925	131.0
	150	39.81	1.9	76	.813	156.0
	175	39.79	2.1	36	.726	181.8

- 1. DEVICE CONDITIONS ARE APPROXIMATE AVERAGE VALUES
- 2. JUNCTION TEMPERATURES BASED ON A CALCULATED THERMAL RESISTANCE (0JA) OF 67°C/WATT FOR MANUFACTURER C AND 79°C/WATT FOR MANUFACTURER B.

FIGURE 16. M38510/10107 (LM118) SUMMARY OF LIFE TEST CONDITIONS

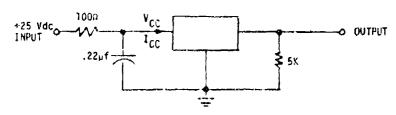


ACCELERATED LIFE TEST CIRCUIT

MANU- FACT- URER	T _A AMBIENT TEMPERATURE ("C)	VCC DEVICE VOLTAGE (VOLTS)	ICC DEVICE CURRENT (MILLIAMPS)	Fd POWER DISSIPATION (MILLIWATYS)	V _O OUTPUT VOLTAGE (VOLTS)	TJ JUNCTION TEMPERATURE (°C)
c	i 50	19.7	2 78	45	7.15	153.0
	175	19.7	2.89	4.7	7,45	178.1
! !	200	19.7	3.21	54	7.06	203.6
e e	150	19.7	2.8?	55	7.25	154.1
	175	19.8	2.72	44	7.25	178.3
	200	19.8	2.67	43	7.25	203.2

- 1. DEVICE CONDITIONS ARE APPROXIMATE AVERAGE VALUES
- 2. JUNCTION TEMPERATURES BASED ON A CALCULATED THERMAL RESISTANCE (θ_{JA}) of 65.7°C/WATT FOR MANUFACTURER C AND 65.5°C/WATT FOR MANUFACTURE? D.

FIGURE 17. M38510/1020! (723) SUMMARY OF LIFE TEST CONDITIONS

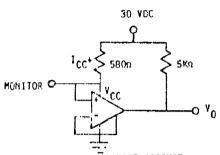


ACCELERATED LIFE TEST CIRCUIT

MANU- FACT- URER	TA AMBIEHT TEMPERATURE (°C)	V _{CC} DEVICE VOLTAGE (VOLTS)	ICC DEVICE CURRENT (MILLIAMPS)	F _d POWER DISSIPATION (MILLIWATTS)	V _O OUTPUT VOLTAGE (VOLTS)	TJ JUNCTION TEMPERATURE (°C)
В	200	24.66	4.25	104	. 561	206.3
	225	24.54	4.55	112	. 460	231.8
	250	20,35	6.51	159	.430	259.6
D	200	24.62	3.99	98	. 892	207.4
	225	24.35	5.09	124	.753	234.4
	250	24.13	7.68	185	.718	264.0

- 1. DEVICE CONDITIONS ARE APPROXIMATE AVERAGE VALUES
- 2. JUNCTION TEMPERATURES BASED ON A CALCULATED THERMAL RESISTANCE (6)A) OF 60°C/WATT FOR MANUFACTURER B AND 75°C/WATT FOR MANUFACTURER D.

FIGURE 18. M38510/10701 (EM109) SUMMARY OF LIFE TEST CONDITIONS



ACCELERATED LIFE TEST CIRCUIT

MANUFACTURER	T _A ANBIENT TEMPERATURE ("C)	VCC DEVICE VOLTAGE (VOLTS)	ICC DEVICE CURRENT (MILLIAMPS)	Pd POWER DISSIPATION (GJELINATTS)	VOLTS)	T JUNCTION TEMPERATURE ("C)
B	200	29.570	.879	24.8	29.78	205.0
	225	29.683	.777	25.7	29.20	230.1
	250	29.628	.848	48.1	25.53	259.6
D	200	29.652	.738	49.0	23.35	210.7
	225	29.6°2	.772	48.1	6.75	235.5
	250	29.657	.798	54.8	10.47	262.0

- 1. DEVICE CONDITIONS ARE APPROXIMATE AVERAGE VALUES.
- 2. JUNGTION TEMPERATURES DASED ON A CAUCULATED THERMAL RESISTANCE $(e_{\rm JA})$ of 200°C/WATT for manufacturer B and 219°C/WATT for manufacturer D.

FIGURE 19. M38510/10304 (LM111) SUMMARY OF LIFE TEST CONDITIONS

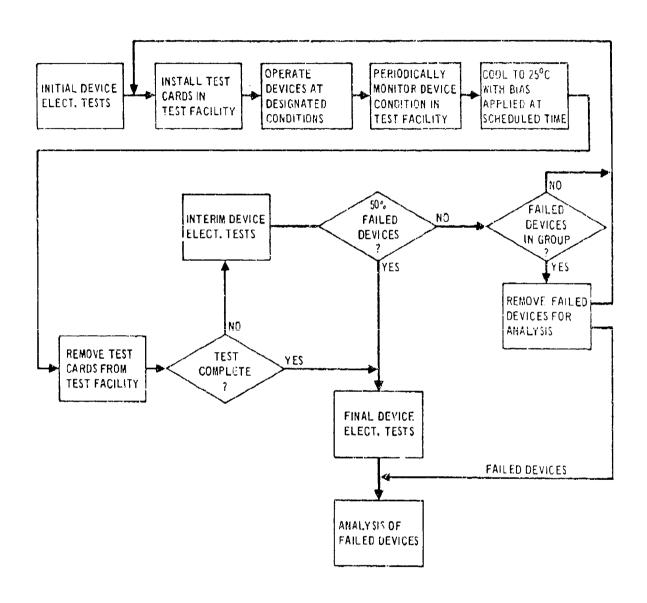


FIGURE 20 . LIFE TESTING SEQUENCE

6-2 ACCELERATED LIFE TEST RESULTS

Accelerated life tests were continued to the 4,000 hour point or to the 70% failure level, and the results are summarized in Table 16. This table shows the cumulative number of devices failing the 25°C dc electrical tests at each measurement point, and the number of devices failing the final 1.25° C and -55° C tests.

TABLE 16. LIFE TEST FAILURE SUMMARY

		NO. OH	MANUFAC-				CUM	ULAT	IVE	NUMB	ER O	F FAI	LURES	AT H	OURS O	F TEST		
P.ART	CELL	TEST	TURER	TEMP	1	2	4	8	16	32	64	128	256	500	1000	2000	4000	FINAL
I.MJ 08A	115	35	A	225	-	-	0	1	2	2	4	10	11	12	17	20	23	26
	114	35	ļ	200	-	-	1	1	2	2	3	3	4	9	13	14	17	17
1	113	35	·	175	1	2	2	4	4	5	6	6	6	7	9	11	16	17
	215	30	В	225	} -	-	18	19	20	20	21	24	25	27	29	-	-	29
ĺ	214	30	}	200	-	-	14	18	18	18	20	22	22	23	26	-	-	29
	213	30		175	11	12	16	18	19	19	19	20	20	23	27	-	-	28
LM118	233	34	В	175	22	23	24	24	25	25	25	26	26	26	28	-	-	28
ŧ	222	34		150	17	22	25	26	26	26	27	27	27	27	30	-	-	33
	221	33		125	0	0	6	15	18	20	21	23	2.3	23	23	-	-	27
	323	34	c	175	1	1	2	2	2	2	3	3	3	3	3	4	8	8
Ì	322	35		150	0	0	1	1	1	1	1	1	1	1	1	2	2	3
	321	34		125	i	1	1	1	1	1	1	2	2	2	3	3	6	6
723	434	35	D	200	-	_	0	0	0	Ç	0	0	û	ύ	0	v	0	0
Ì	433	34		175	-	-	1	1	1	1	2	2	2	2	2	2	3	3
	432	35		150	-	-	0	0	0	0	0	0	0	0	0	0	0	0
	334	30	С	200	-	-	0	0	0	0	0	O	0	0	0	6	6	8
]	333	35	ì	175	-	-	0	0	0	0	0	0	0	0	Ü	0	O	0
	332	35		.150	-	-	0	0	0	0	O	0	0	0	0	0	0	O
LM109	256	.35	В	250	-	_	Ú	0	0	0	0	1	2	ĉ	2	2	3	3
	255	35		225	-	-	0	1	1	1	2	2	2	2	2	2	3	3
	254	35	1	200	-	-	۵	0	Ú	0	0	O	0	2	2	2	3	3
	456	35	D	250	-		2	2	3	3	3	3	3	3	3	4	4	4
	455	35		225	-	~	0	0	1	1	1	1	1	1	1	2	2	2
	454	3 5	-	200	-	-	2	2	2	3	3	3	3	3	3	3	3	3
LM111	24€	35	R	250	-		4	5	6	11	12	14	16	19	23	-	-	24
	245	35	1	225	-	-	2	2	2	3	8	10	16	22	25		-	25
	244	35		200	-	-	0	0	O	Q	0	3	4	16	25	-	-	29
j	446	35	٥	250	-	-	O	2	2	5	5	5	12	14	34	-		34
	445	33		225	-	-	1	6	7	12	12	12	16	19	29	-	-	29
	444	35		200	-	-	0	1	1	2	9	9	18	19	35	-	•	35

7.0 FAILURE ANALYSIS

All devices failing an interim or final electrical test during step stress and life testing were analyzed to determine the failure mode, mechanism, and probable cause. However, only a limited analysis was performed for those few devices that exhibited a random, isolated failure mode and most of the devices that exhibited parametric failures at +125°C only. Summaries of the failure analysis findings for each manufacturer's device type are shown in Tables 17 through 21. Complete details of the failure analysis procedures and findings are contained in Appendix F.

TABLE 17. MIL-M-38510/10107 (LM118) FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS			LURES AND	: 15°E OF E				
B. FAILURE MODE		HANUF ACTU				HUF AC TUR		
E. CAUSE OF FAILURE	STEP STRESS	ALCE	LERATED LI		STEP STRESS	ACCE	LERATIO LI	F [
E. GOOT OF PATEUR	31,623,	125°C	150°C	175°C	318233	125°€	150°C	175°C
A. VIO AND/OR PORR B. CHANNEL CURRENT FROM RIS TO THE SUBSTRATE C. IMPERITOR OF THE ESSISTOR TUB DUE TO CHANGE MIGRATION D. MUBILE IONS OR CHARGES IN THE PASSIVATION	3%125°C 20;50°c	584 968 3819 2832 1864 28128	1541 562 364 166 1664 1*81000	22 0 1 102 134 1016 101000				
A. 1 ₁₀ P V _{CM} = -15V B. V+ 10 IPPUT CHANNEL CURRENT C. PKDBABLY INVERSION OF THE C-B JUNCTION OF THE INPUT TRANSISTOR D. MOBILE IONS IN THE PASSIVATION			381050 1*81050			194000		164
A. 1 OF 1B B. LOW CAIN IN INPUT TRANSISTOR C. PPOGABLY DEPLETION OF THE DASE D. MOBILE IONS OF CHARGES IN THE PASSIVATION				10128 101000		161 264000		19200
A. V ₁₀ LATCHED UP B. MELTED STRIPES AND SHORTED JUNCTIONS C. PRUBADLY THERMAL RUNAWAY OF C1 D. UNKNOWN		•			19200°C 19250°C 29275°C			192 2 0 4000
A. V ₁₀ LATCHED UP B. SHORTED CAPACITOR C. DIELECTRIC BREAKDOWN D. DLFECT IN DIELECTRIC SIG						10128	1#4 182000	26400
A. V ₁₀ EATCHED UP B. OPEN STRIPE OR SHORTED JUNCTION C. ELECTRICAL OVERSTRESS D. TEST ERROR		164				181000	1*84000	
A. V ₁₀ AND PSRR {RECOVERED UPON DILIDDING}								1964
A. PD B. RORE C. NOME U. TEST ERROR (INITIALLY FAILED)		4*@1000	201 1*01000					
TUTAL NUMBER OF FAILED PAPTS	5	27	33	28		6	3	8

TABLE 18. MIL-M-38510/10104 (LM108A) FAILURE ANALYSIS SUMMARY

A.	FAILED PARAMETERS OF CYMPTOMS	QUANTI	TY OF FAL	LURES AND	TIME OF F	ASLURE (F	IOURS) BY	TEST CELL	
8.	FAILURE MODE		MANUF ACTU	RER B		N	UNUF ACTURE	R A	
с.	FAILURE MECHANISM	STEP	ACCE	LERATED L	IFE	STEP	ACCEL	ERATED LI	Fξ
۸,	CAUSE OF FAILURE	STRESS	175°C	200°C	225°C	STRESS	175°C	200°C	225 ° C
8.	V ₁₀ AND/OR A _{VS} CHANNEL CURRENT FROM R7 TO THE SUBSTRATE INVERSION OF THE R7 RESISTOR TUB MOBILE IONS OR CHARGES IN THE PASSIVATION	10125°C 10150°C 10175°C 10175°C	1091 192 494 298 1916 39500 491600 1*81000	1464 368 2664 20128 301000 3*01000	1884 188 1816 1864 38128 18250 28500 281000				
3 .	Y ₁₀ LATCHED UP MELTED STRIPES AND SHORT'D JUNCTIONS THERMAL RUMAWAY AT US UNKNOWN						195000 292000 484000	19256 49500 491000 192000 394000	108 3064 30128 10256 10500 30100 20200 30400
₽.	AVS NOT DETERMINED (RECOVERED) SURFACE INSTABILITY PROBABLY IONIC CONTAMINATION						191 198 291000 192000	10500	20100 10200 010400
B. C.	I ₁₀ AND/OR I ₁₈ PROBABLY DEGRADED IMPUT TRANSISTORS PROBABLY CHARGE ACCUMULATION TEST ANOMALY (STATIC DISCHARGE)		101 10128	168 16500			192 1932 1064	194 1616 1664	1016 20128
÷12	STO FAILURES AND RANDOM FAILURES - NOT ANALYZE	D IN DETAIL							
٩.	¥ ₁₀ € +125°C UNLY						194000		1840
۸.	110 0 4 125°C ONLY								1940
۸.	I _{OS} (-) (RECOVERED WHEN LEFT ON TEST)						168		
					1	ı	1		1

TABLE 19. MIL-M-38510/10701 (LM109) FAILURE ANALYSIS SUMMARY

	FAILED PARAMETERS OR SYMPTOMS	QUANTIT	OF FAILU	RES AND TIME O		RS) BY TI	EST CELL
_	FAILURE MODE			ACÇELERAT			
	FAILURE MECHANISM	L.—.—	IUF AC TURER			N'ACTURER	
D.	CAUSE OF FAILURE	200°C	225*C	250°C	200°C	225°C	250°C
A.	OPEN PIN				19500	1864	10250
В.	LIFTED WERE BUND AT THE POST	•		j		194000	
c.	KINKENDALL VOIDING IN AUAI	j '		}			Ì
٥.	EXCESSIVE AUA12 GROWTH DURING BONDING						l 1
Α,	OPEN PIN 1 OR 3		102000			196	
8.	BROKEN EXTERNAL LEAD	1	,				}
с.	ACCHANICAL OVERSTRESS	1	İ				1
D.	MI SHANDLING	-			Ì		_
A.	OPEN PIN 3				194000		10120
в.	BROKEN EXTERNAL LEAD	ļ	ĺ		[1
c.	AU LEACHING	ĺ		1	1	Į	Į.
D.	TIN SOLDER			-	į	ļ	
۸.	Δ1 _{SCD} [13]	204	1016	294			194000
	NONE	1864	j	1016	1	<u> </u>	1
С.	NUNE	Ì]	182000	Ì		ì
O.	INTITIALLY FAILED OR MARGINAL						ì
RAI	NOOM FAILURES - NOT ANALYZED IN DETAIL					4	
Α.	V _{OUT} [4] (ONLY MARGINALLY FAILED)				16500		
TO	TAL NUMBER OF FAILED PARTS	3	2	4	3	3	3

TABLE 20. MIL-M-38510/10201 (723) FAILURE ANALYSIS SUMMARY

	FAILED PARAMETERS OR SYMPTOMS FAILURE MODE	QUANTITY	OF FAILUR	ACCELERAT	F FAILURE (HO	URS) BY T	EST CELL
	FAILURE MECHANISM	· MAN	UF ACTURER			UF ACTURER	С
٥.	CAUSE OF FAILURE	150°C	175°C	500 °C	150°C	175°C	200°C
₿.	SCD NONE NONE						602000
	TEST SET ORIFT				ı		
8. C.	VRE. OR VR LINE [1] + VR LOAD [4] @ -55°C NONE NONE FROBABLY AN INTERMITTENT TEST SOCKET						294000
₿. ¢.	I _{OS} MYT DETERMINED SURFACE INSTABILITY + INITIALLY MARGINAL MOBILE CONTAMIMANT IONS		164 1624				
RAI	NDOM FAILURES - NOT AMALYZEV IN DETAIL						
A.	VR LINE [1] (ONLY MARGINALLY FAILED)		184000				Ţ
70	TAL NUMBER OF FAILED PARTS	0	3	0	0	0	8

TABLE 21. MIL-M-38510/10304 (LM111) FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS		Y OF FAIL		TIME OF FA	·						
8. FAITURE MOJE		MANUF ACTUR			MANUF ACTURES D						
C. FAILUPE MECHANISM D. CAUSE DE FAILURE	STEP	ALU:	LERATED LI	P	STE? STRESS	ACCELERATED ; IFE					
and the second s	3,403	200°C	.25°C	250°C	314577	200°C	225°C	250°C			
A. V ₁₀					1#225°C	1.08	3€6				
N. LOW her IN O4	} ;	301000	194		10275°C	1032	1016	198			
C. INVERSION OF THE BASE OF Q4	<u> </u>		1964		}	SUK4	5032	3032			
D. PROGABLY JOHIC CONTANINATION	- 1 .		191000		ĺ	96 , 56	40256	7025			
	1)	12500	39500	1050			
)			1	1691000	1001000	20010			
A. 1 ₁₀	10175°C	10138		344	16500,0						
8. LOW h _{FF} IN 32	20275°C	10256	184	1916	1	1964	194	106			
C. SURFACE INSTABILITY AND BULK-RELATED		126590	1032	5932			1	1050			
AC CHANTSHS	1	661000	4964	1964	}	Ì]	1			
D. FRODABLY IONIC CONTAMINATION	1		29128	20128	ì	1	1	1			
2007	j .	1	60256	29256	}	1	1	1			
	1	1	58500	38500	1	1	1	1			
	İ		291000	301000							
A. I ₁₈	20175°C										
B. MARE	ĺ	}	1	İ	ł	1	1	ł			
C. PORE	1	i	Ì	1	1	İ	j				
D. V _{CH} TOO RIGH					<u> </u>			<u> </u>			
A. 1 ₀		19128		164							
#, DEGRADED QLS COLLECTOR - SUBSTRATE	1	1	}	198]	ì	1	1			
Droce		1	<u> </u>		1	ļ.	į .	1			
C. PAOBABLY INVERSION OF THE COLLECTOR		1		Į	1	l		1			
U. FRUBABLY CATION CONTAMINATION			<u> </u>	<u> </u>		<u> </u>	<u></u>				
+125°C UMEY FAILURES AND RANDOM FAILURES - NOT A	ID NT CESY JAKA	ETAIL									
A. CHR (RETEST OK)]			1,064	298				
A. A _{VC} (RECUYERED)		10128	19500								
A. Ayc # +125"C DHLY		401900		181000							
A. Y _{QL} [30]				191000	\						
TOTAL HUMBER OF FAILED PARTS	5	29	25	24	3	35	29	34			

8.0 DATA EVALUATIONS AND CORRELATIONS

Evaluations and correlation of the data generated during the program were performed to determine device aging characteristics. This was accomplished through comparisons of the types of failure modes observed in each test, plots of failure distributions, Arrhenius model evaluations, and calculations of use temperature failure rates. The determination of failure distributions, Arrhenius model parameters, and usc temperature failure rates generally followed published techniques [2], [3], and [4].

8.1 FAILURE MECHANISM IDENTIFICATION

The types of failure mechanisms generated for each device type during step-stress and accelerated life testing are simmarized in Table 22. The first three mechanisms (inversion of an N-type tub, collector or base, depletion or inversion of a P-type base, and surface instability mechanisms which could not be traced to a specific mechanism) are all surface related mechanisms. These surface related mechanisms accounted for 75% of the total number of device failures. The second largest group of failures (5%) was attributed to a localized thermal runaway mechanism. This mechanism was time-temperature dependent but the cause of this dependency could not be determined. Only a small percentage of devices (approximately 1% for each mechanism) failed due to dielectric breakdown (oxide related), Kirkendail volding (wire bond related), and gold leaching (package related). The failure mechanisms for a small percentage (3%) of the failures are classified as unknown because either the devices had recovered before the failur rechanism could be established, or the devices were not investigated since the devices exhibited only a single marginally out-of-tolerance parameter, or a single parametric failure at 125°C only, or a random isolated type of failure.

A summary of the types of defects observed and the suspected defect causes is shown in Table 23 for each manufacturer's device type. The absolute cause of failure could not be positively determined in many cases, consequently many of the failures identified as process-related may ultimately or indirectly involve the design or materials of the device. Nevertheless, the failures

TABLE 22. FAILURE MECHANISM SUMMARY

	LMJ 18			LM108A				723				LM109				LM111					
FAILURE MECHANISM		MER B MER C		MFR A M		MFF	FR 8 P		MFR C		MER D		₹ В	HFR D		MFR B		MFR	0		
		₩Q.	*	NO.	x	NQ.	7.	אח.	3	MQ.	3	NO.	Ä	NO.	×	no.	2	NO.	2	NO.	2
1.	INVERSION OF N-TYPE TUB, COLLECTOR, OR BASE	83	89	2	10			86	96									67	81	5	5
2.	DEPLETION OR INVERSION OF 2-TYPE BASE	2	2	4	19													6	7	93	92
3.	SURFACE INSTABILITY			•		10	17					2	67								
4.	THERMAL RUNAWAY			7	33	37	62														
5.	DIELECTRIC BREAKDOWN			5	23																
6.	KIRKENDALL VOIDING													4	45						1
7.	AU LEACHING			ļ)	}			2	22))				
8.	STATIC CHARGE ACCUMULATION					ç	15	4	4					ľ							
9.	MECHANICAL OVERSTRESS								}]]		2	22	1	11	Ì '			
10.	ELECTRICAL OVERSTRESS	1	1	2	10	1	}			Ì	1				1	1	Ì				ì '
11.	NONE (TEST SET ERROR)	7	8])	Ì		}	8	100)		l	1	8	89	2	5		1
12.	NUKNOHN			1	5	4	6					1	33 	1	11			8	10	3	3
	TOTAL.	93	100	21	100	60	100	90	100	8	100	3	100	9	100	9	100	83	100	101	100

A Specific Mechanism Vaknown

TABLE 23. DEFECT/CAUSE SUMMARY

		NUMBER OF FAILER DEVICES													
PRIMARY DEFECTS AND CAUSES		LH1	18	LM2	QBA	72	3	[H]	09	LM111					
		HFR B	MFR C	MFR A	HFR B	NFR C	MFR D	MER B	HIFR D	MFR B	MERD				
DEFEC	T CATEGORY									1					
1.	SURFACE PELATED	85	6	10	85	c	2	3	9	73	98				
2.	OXIDE RELATED	٥	5	0	6	C	0	Ü	C	0	0				
3.	WIRE BOND RELATED	0	0	0	0	G	o j	4	0	0	0				
4.	PACKAGE RELATED	ŭ	0	0	0	0	0	2	0	l o	0				
5.	ELECTRICAL OVERSTRESS	1	2	9	4	0	0	0	0	0	0				
6.	TEST EPROR	?	O	0	0	8	υ	2	9	2	0				
7.	UNUEFINED	0	8	41	٥	0	1	i	υ	8	3				
	TOTA! S	93	21	6.0	90	8	3	9	9	83	101				
CAUSE	CATEGORY						<u> </u>								
1.	PROCESS PELATED	85	11	10	86	0	2	4	0	73	98				
2.	DESIGN RELATED	α	0	0	0	0	0	0	0	0	0				
3.	MATERIAL RELATED	Q	0	0	0	0	l e	2	9	0	С				
4.	WORKMANSHIP RELATED	0	0	0	a	0	0	0	l u	0	0				
5	TEST RELATIO	8	2	9	4	٤	0	2	9	2	0				
6.	UNKNOWN	. 0	Łļ.	41	С	n	1	1	n	8	3				

attributed to process-related problems probably can be reduced by a tightening of process controls.

8.2 FAILURE TIME CALCULATION

The failed devices exhibited out-of-tolerance parameter values or, in some cases, catastrophic failures. Thus, the parametric data was examined for time dependent degradation and, where feasible, interpolation methods were used to determine the actual device failure time. Where the interpolated failure times were gathered about the measurement times or where the device failed catastrophically, the midpoint between the last two measurement times was used as the estimated failure time.

8.3 FAILURE DISTRIBUTIONS

Distributions of the times to failure were determined for each manufacturer's device type whenever sufficient failure data was available. The failures due to test-set related problems, and those failures that occurred only at 125°C and -55°C were not included in these analyses. In all cases, the failure time distributions were assumed to be either single lognormal distributions, or bimodal distributions that could be represented by two lognormal distributions. The bimodal distributions were represented by two lognormal distributions [6], an early distribution of failures (freak), and a later distribution of failures (main). This bimodal failure distribution is

$$\begin{aligned}
& \text{Cdf {life}}_{\text{TOTAL}} = \left\{ \frac{1}{\sigma_F \sqrt{2\pi}} \int_0^t \frac{1}{t}, & \exp\left\{ -\frac{\left(\ln t' - \mu_F\right)^2}{2\sigma_F^2} \right\} dt' \right\} & (x_F) \\
& + \left\{ \frac{1}{\sigma_{ii}\sqrt{2\pi}} \int_0^t \frac{1}{t}, & \exp\left\{ -\frac{\left(\ln t' - \mu_M\right)^2}{2\sigma_M^2} \right\} dt' \right\} & (x_M)
\end{aligned}$$

where

 μ_F . In (median life of the freak distribution)

 $\sigma_{\rm F}$ = standard deviation of the freak distribution

 $\mu_{\rm M}$ = ln (median life of the main distribution)

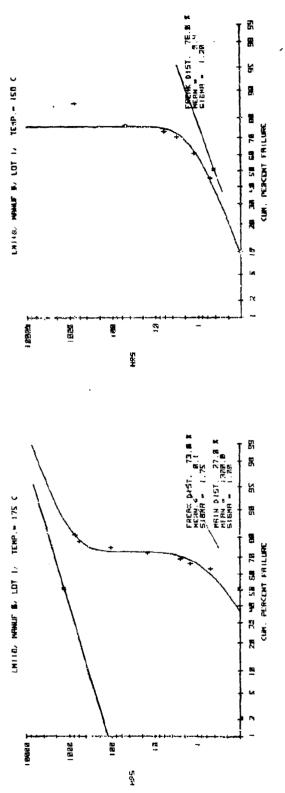
 $\sigma_{\rm K}$ = standard deviation of the main distribution

- $%_{F}$ = the percentage of the total population that is described by the freak distribution
- $%_{M}$ = the percentage of the total population that is described by the main distribution
- t = use time

Then the graphic result was used with equation (1) and the calulated probability was compared to the test probability at each failure time. From this starting point the values of the unknowns in equation (1) were iterated and the probabilities compared until plots of the resulting equation appeared to provide a good representation of the observed data.

8.3.1 <u>LM118 Failure Distributions</u> - The primary failure mechanism for Manufacturer B's LM118 devices was inversion of a resistor tub, most probably caused by either the separation of mobile ionic species in the fringing field of the reverse biased junction, or electron drift in the fringing field along defects in the glass/insulator interface. Also included in the failure distributions were failures due to inversion of the collector-base junction of an input transistor and failures due to depletion of the base region of an input transistor. Both mechanisms are suspected to be caused by mobile ions or charges in the passivation layers. The failure distributions for these surface related mechanisms at each test temperature are shown in Figure 21. A bimodal distribution is indicated but the data was only sufficient to determine the main distribution median life at the highest test temperature (175°C). Even for this temperature, there are only a few data points, and the actual failure distribution of the main population cannot be accuracely determined.

Only a small percentage (16.5%) of Manufacturer C's LM118 devices failed and the failures were divided into the following time-temperature dependent mechanisms: a) inversion of an input transistor, b) depletion in the base of a transistor, c) thermal runaway at C1, and d) dielectric breakdown in a capacitor. There were insufficient data to permit a valid evaluation of the Manufacturer C failure distributions.



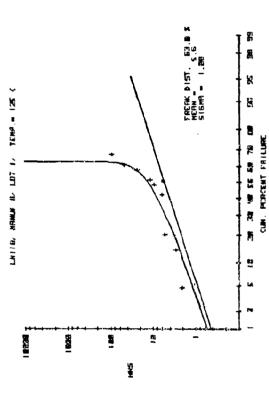
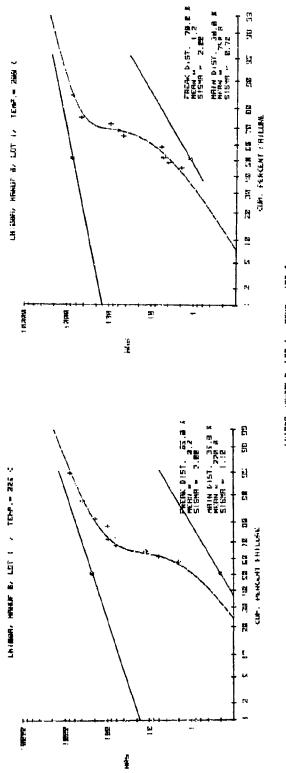


FIGURE 21. MANUFACTURER B LM118 FAILURE DISTRIBUTIONS - RESISTOR TUB INVERSION

8.3.2 <u>LM108A Failure Distributions</u> - The primary mechanism of failure for Manufacturer B's LM108A devices was also channel current from a resistor to the substrate due to inversion of the resistor tub. The most probable causes of this mechanism were the same as those previously mentioned for Manufacturer B's LM18 devices: either the separation of mobile ionic species in the fringing field of the reverse biased junction, or electron drift in the fringing field along defects in the glass/junction interface. The failure distributions for this mechanism are shown in Figure 22. The distributions are bimodal and the freak population accounts for approximately 65% to 70% of the total population.

The primary failure mode for Manufacturer A's devices was thermal runaway of PNP transistor Q6. Several devices also failed the gain test (A_{VS}) , but these devices were left on test and most of the devices recovered. Three of the gain failures later failed at the 2000 hour test point due to thermal runaway and are included in the failure distributions. The other gain failures are not included, since the gain measurements are not representative of actual gain, and are not necessarily indicative of failure, as was discussed in Section 4.0. The failure distributions for the thermal runaway mechanism are shown in Figure 23, and are single lognormal distributions. Although thermal runaway would normally be considered a temperature dependent only mechanism, the failure distributions do indicate a time-temperature dependency. The exact cause of this dependency was not established, but is probably linked to the bulk degradation of the emitter of Q6.

8.3.3 LM111 Failure Distributions – The majority of Manufacturer B's LM111 failures were due to excessive I_{10} and the failures were attributed to two mechanisms, a surface related (reversible) mechanism which predominated at 200°C and a bulk related (nonreversible) mechanism which predominated at 225°C and 250°C. Also included in the failure distribution plots were the two other surface related mechanisms, inversion of the base of an input transistor, and inversion of the collector region in an output transistor. Both mechanisms were probably caused by ionic contamination in or on a passivation layer. The 25°C collector gain (A_{VC}) failures were excluded from the distributions due



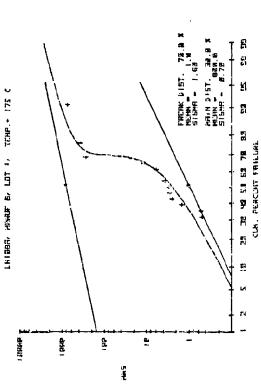
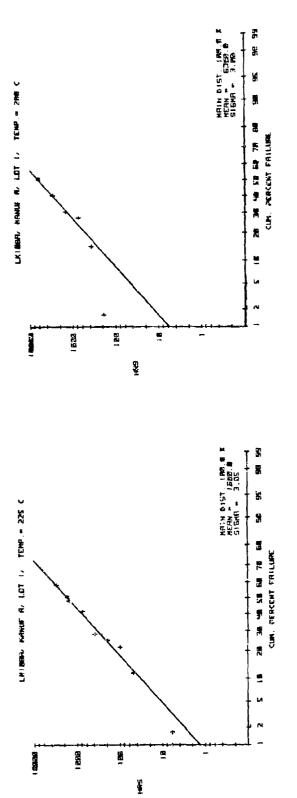
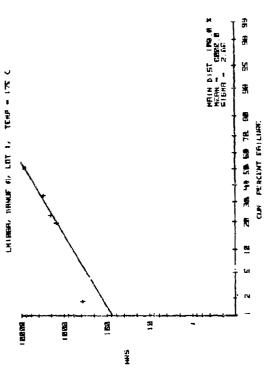


FIGURE 22. MANUFACTURER BIMIOSA FAILURE DISTRIBUTIONS - RESISTOR TUB INVERSION





MANUFACTURER A LM108A FAILURE DISTRIBUTIONS- LOCALIZED THERMAL RUNAWAY FIGURE 23.

to the nonlinearity of the gain measurements. The resulting failure distributions shown in Figure 24 indicate single lognormal distributions at each test temperature. The difference in standard deviation (sigma) between the 200°C plot and the higher temperature plots supports the failure analysis findings suggesting different mechanisms predominating at those temperatures.

The primary mechanism for Manufacturer D's LM111 devices was an inversion of the base of an input transistor, a surface related mechanism most probably caused by ionic contamination in or on a passivation layer. Also included in the failure distribution plots were four ${\rm I}_{10}$ failures due to the surface instability and bulk mechanism discussed above. The failure distribution plots indicate a bimodal distribution at all test temperatures as shown in Figure 25.

8.3.4 LM109 and 723 Failure Distributions - Insufficient failure data was generated in the accelerated life tests of both the 723 and LM109 devices to permit evaluation of the failure distributions.

8.4 AGING CHARACTERISTICS

Sufficient multiple temperature data was generated during the accelerated life tests of the Manufacturer B LM118 and both manufacturers' LM108 and LM111 devices to evaluate aging characteristics for these device types. The Arrhenius reaction rate model [4] was found to provide a good representation of the aging characteristics for the freak and main device populations, and was used to relate median lifetime and junction temperatures as follows:

$$t_{50\%} = A \exp\left(\frac{E_A}{kT}\right) \tag{2}$$

where

 $t_{E,\Omega M}$ = freak or main population median lifetime at a junction temperature

A = A constant

 E_A = Experimental activation energy - eV k = Boltzman's constant - 8.617 x 10^{-5} eV/Kelvin

T = Absolute junction temperature - Kelvin

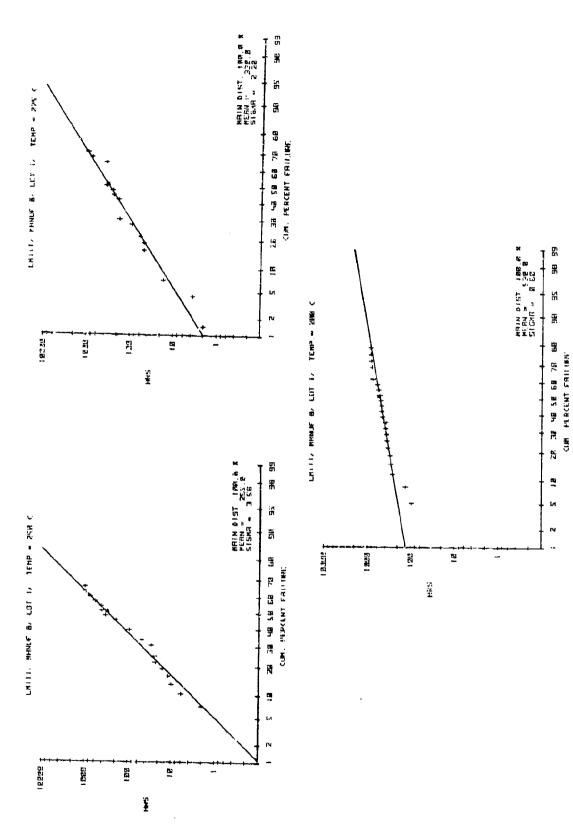
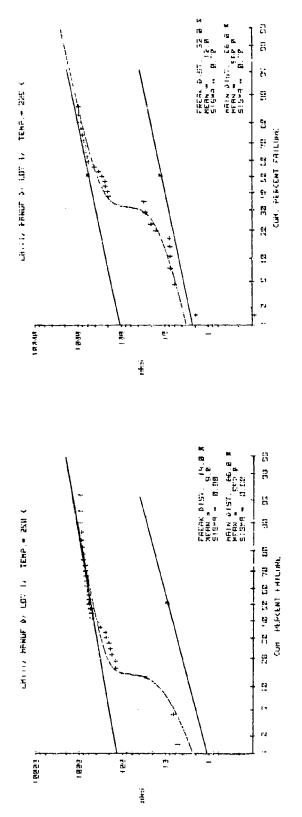
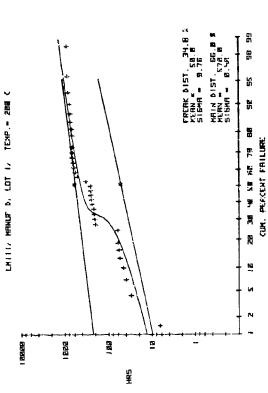


FIGURE 24. MANUFACTURER B LM111 FAILURE DISTRIBUTIONS - SURFACE INSTABILITY & BULK RELATED





MANUFACTURER D LM111 FAILURE DISTRIBUTIONS - TRANSISTOR BASE INVERSION FIGURE 25.

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The linear transform of this equation is

$$\ln t_{50\%} = \ln \Lambda + \frac{L_A}{k} \left[\frac{1}{T} \right]$$
 (3)

The transformed Arrhenius equation was evaluated using a linear regression analysis that assumes the junction temperature is a known value and $\ln t_{50\%}$ is the only variable [7], [8].

- 8.4.1 <u>Manufacturer B's LM118 Devices</u> The Arrhenius piot for Manufacturer B's LM118 freak population failures is shown in Figure 26. The activation energy was calculated to be 1.24 eV for the surface instability mechanisms responsible for the failures. The freak population consisted of approximately 72% of the sample size. There was insufficient data to calculate the main population activation energy.
- 8.4.2 <u>Manufacturer A's LM108A Devices</u> Sixty-two percent of Manufacturer A's LM108A device failures were attributed to thermal runaway at the Q6 transistor. At elevated temperatures the current in the transistor reached excessive levels, resulting in catastrophic damage to the device. Normally this would not be considered a time-temperature dependent mechanism, but evaluation of the failure data indicated that the failures were time-temperature dependent as shown in Figure 27. The activation energy for this mechanism was calculated to be 0.61 eV.
- 8.4.3 <u>Manufacturer B's LM108A Devices</u> Manufacturer B's LM108A time-temperature related device failures were due to inversion of a resistor tub. The Arrhenius plot for this failure mechanism is shown in Figure 28. The activation energy was calculated to be 0.61 eV for the freak population and 0.49 eV for the main population. Both these activation energies differ from the 1.24 eV activation energy calculated for the Manufacturer B LM118 freak population with a similar failure mechanism. The failure mechanism in both devices was suspected to be either separation of the mobile ionic species in the fringing field of the reverse biased junction, or electron drift in the fringing field

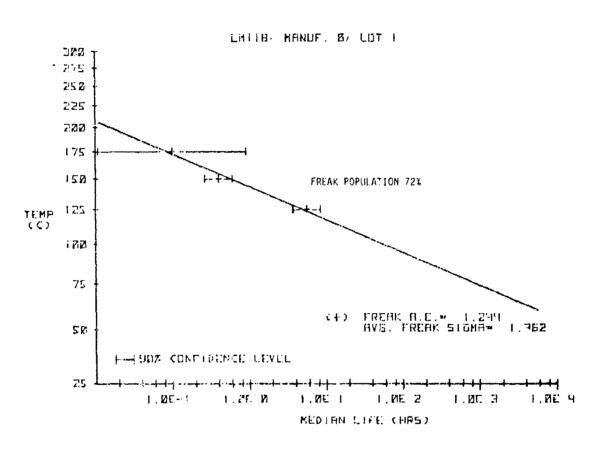
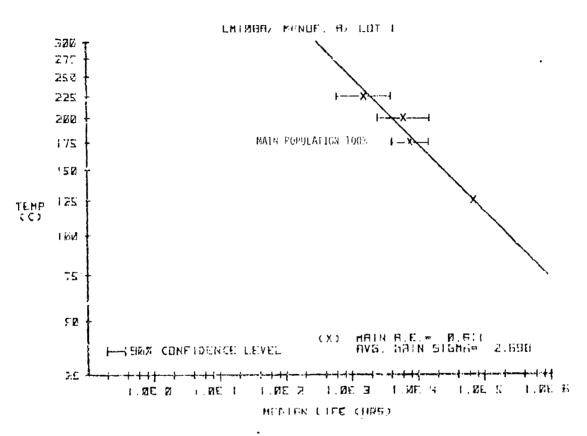


FIGURE 26. MANUFACTURER B 19118 ARRHENIUS PLOT - RESISTOR TUB INVERSION



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FIGURE 27. MANUFACTURER A LMIUSA ARRHENIUS PLOTS - LOCALIZED THEPMAL RUNAWAY

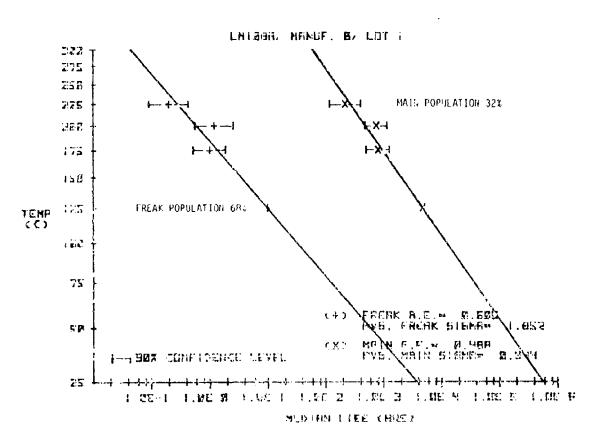


FIGURE 28. MANUFACTUR R R EMIOSA ARRHENIUS PLOTS - RESISTOR TUB INVERSION

along defects in the glass/junction interface. Thus, the difference in activation energies is possibly due to one mechanism predominating in one device and the other mechanism predominating in the other device.

- 8.4.4 Manufacturer B's LM111 Devices The Arrhenius plot shown in Figure 2S is for the bulk failure mechanism which predominated at the 225°C and 250°C temperatures. This mechanism exhibited an apparent activation energy of 0.10 eV. Also shown on the plot is the median life of the 200°C failures which were attributed to a surface related mechanism. Since no 200°C life test failures were attributed to the bulk related mechanism, the Arrhenius plot for this mechanism should not be extended below 225°C. However, the exact nature of both the bulk and surface related mechanisms could not be determined, and it is possible that the two mechanisms are related. Therefore, as a means of establishing a conservative estimate of use-temperature failure rates, the Arrhenius plot has been extended below 225°C.
- 8.4.5 Manufacturer 0 c ! Mill Devices The freak population accounted for an average of 28% of Manufacturer D's LM111 devices and exhibited an activation enargy of 0.74 eV as shown in Figure 30. The main population exhibited a very low activation energy of 0.01 eV. This indicates a non-temperature dependent failure mechanism. Approximately 50% of the failures due to this mechanism occurred between the 500 and 1000 hour measurement points at each test temperature. Also, the calculated median lifetimes of the main population at each test temperature were all approximately 600 hours. An examination of the parameter drift data was made in an effort to determine the reason for this low activation energy. The value of the failing parameter (${
 m V}_{10}$) was plotted versus test time as shown in Figure 31. It was noted that the parameter value would sometimes increase if the device were left on bias at 25%, for a period longer than 24 hours prior to being electrically tested. However, the overall drift of the devices does appear to be independent of temperature. The failure analysis of the devices determined that the morbanism was bake recoverable and that the failures were due to a garm mismatch in the input transistors. most probably caused by ionic contamination. This rechanism is generally time-temperature dependent, but there were no other anomalies that would account for the temparature independent nature of the failures.

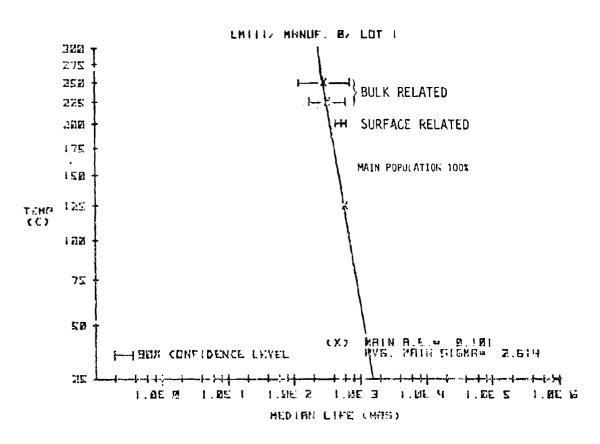


FIGURE 29. MANUFACTURER B LMTTT ARRHENIUS PLOTS - SURFACE
INSTABILITY AND BULK RELATED

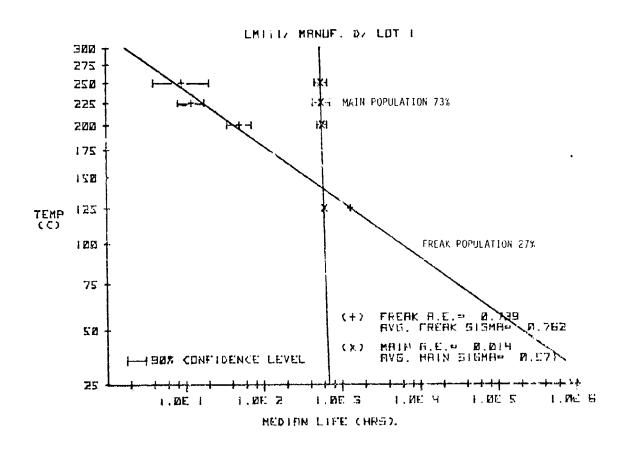


FIGURE 30. MANUFACTUPER D LMT11 ARRHENIUS PLOTS - TRANSISTOR BASE INVERSION

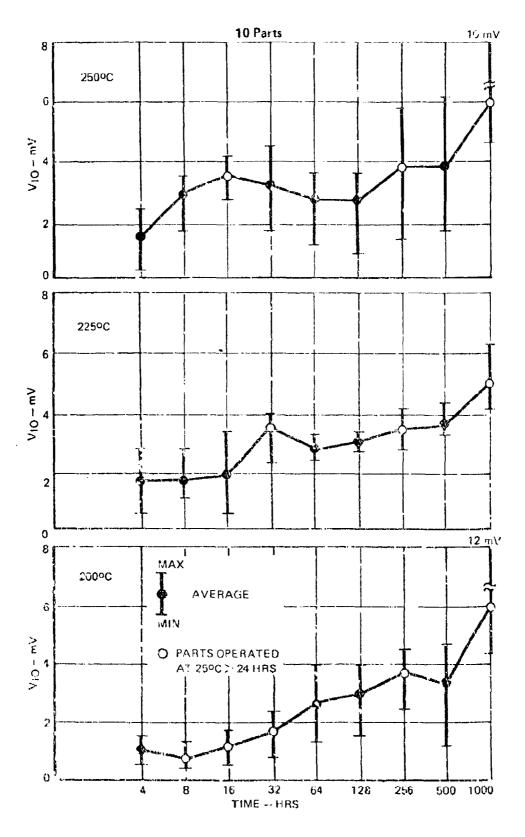


FIGURE 31. MANUFACTURER D LM111 OFFSET VOLTAGE PARAMETER DRIFT

8.5 FAILURE RATES

Use-temperature failure rates were calculated using the values shown in Table 24 for Arrhenius model parameters (constant "A" and activation energy " E_A "), average value of lognormal distribution standard deviation and percent freak and main population. The failure rate for a single distribution is defined as [9]

$$\lambda(t) = \frac{f(t)}{R(t)} \tag{4}$$

where

 $\lambda(t)$ = the instantaneous failure rate at time

f(t) = the failure density at time t

R(t) = the reliability at time t.

Also, a lognormal failure rate for a single distribution is defined as [10]

$$\lambda(t) = \frac{\frac{1}{t \sigma \sqrt{2\pi}} \exp \left\{-\frac{\left(\ln t - \mu\right)^{2}\right\}}{\frac{2\sigma^{2}}{\sigma^{2}}}$$

$$\frac{1}{\sigma \sqrt{2\pi}} \int_{t}^{\pi} \frac{1}{t} \exp \left\{-\frac{\left(\ln t - \mu\right)^{2}\right\}}{2\sigma^{2}} dt'$$
(5)

where

μ= ln (median life)

 σ = the standard deviation.

Assuming that an Arrhenius equation defines the median life at a junction temperature provides the following temperature dependent, lognormal failure rate:

$$\frac{1}{t \, \sigma \, \sqrt{2\pi}} \, \exp \left\{ -\frac{\left[\ln t - \left(\ln A + E_A/k \, T \right) \right]^2}{2\sigma^2} \right\} dt'$$

$$\frac{1}{\sigma \, \sqrt{2\pi}} \int_{t}^{\infty} \frac{1}{t'} \, \exp \left\{ -\frac{\left[\ln t' - \left(\ln A + E_A/k \, T \right) \right]^2}{2\sigma^2} \right\} dt'$$
(6)

TABLE 24. SUMMARY OF FAILURE RATE PARAMETERS

	AVS	3 2.70	3	1	2.42	0.57
KAIN	∢.	1.30 × 10 ⁻³	3.13 × 10 ⁻³	•	1.03	4.07 × 10 ²
	رن م جر ک	0.63	0.43	◀	0.10	0.01
	AVG		1.92	1.36	1	0.76
FREAK	¥	ı	2.15 x 10 ⁻⁷	8.55 x 10-16	3	5.68 x 10 ⁻⁷
	(eY)	ı	0.61	1.24		0.74
	AUG I	165	32	78	100	73
	ACC X FREPK	0	68	72	0	23
	PAILURE PECHANISM	THERMAL KUMPYAY AT QE	RLSISTOR TUB INYERSION	AELLSTOR TUB INTERSTON	TRANSISTOR BASE	HUNERSTON BULK RCLATED
	9. 9.	r:	96	~	œ	c
	PARIT.	LM108A	LP108A	LM118	LMIII	

NOTE: A INSUFFICIENT DATA TO CALCULATE PARTALTER VALUES.

For a bimodal distribution consisting of two lognormal failure rates, the total failure rate is defined as

$$\lambda(t)_{TOTAL} = (t)_{freak} (\% freak) + (t)_{main} (\% main)$$
 (7)

These techniques were used to calculate the maximum instantaneous failure rates shown in Table 25 — Comparison of the 125°C and 50°C failure rates illustrate the value of junction temperature derating to achieve improved failure rates for the predominant failure mechanisms. Additional factors for secondary failure modes must be included in the total device failure rate prior to using the failure rates for reliability estimates.

The failure rates shown are for device junction temperatures of 125°C and 50°C. The failure rates are based on the predominant failure mechanism for all devices. The devices were burned-in by the manufacturer for 168 hours at 125°C. The specified additional hours of 125°C burn-in shown in Table 25 would be required to eliminate 99.9% of the freak population. Removal of 99.9% of the freak population can be assumed to constitute removal of all freak devices. An additional 271 hour burn-in at 225°C for Manufacturer B's LM108A devices would result in an improvement in failure rate, but would eliminate 22% of the main population, and since the freak population consisted of 68% of the sample, this would result in 75% of the devices being removed. An additional burn-in of 30 hours at 175°C would remove the freak population cf Manufacturer B's LM118 device, but there was insufficient data to evaluate the main population failure rate. Also the freak population accounted for 72% of the sample size. An additional burn-in for Manufacturer D's LMILL device would actually increase the failure rate due to the fact that the median lifetime of the main population is actually less than the freak population at temperatures less than 150°C. Additional burn-in for those devices which exhibited a single lognormal distribution would not result in improved failure rates without sacrificing a high percentage of the total population. In general, additional burn-in is not recommended since either it is not cost effective, or the failure rates cannot be greatly improved.

TABLE 25. FAILURE RATE SUMMARY

		MUMIXAM					
		WITHOUT BURN-IN		WITH B	BURN-IN CONDITIONS		
DEVICE	MFR	125°C	50°C	125°C	50℃	TIME (HRS)	(°C)
1.M108A	A	8.02 x 10 ⁻⁵	2.27 x 10 ⁻⁸	Δ	•	•	-
LM108	В	8.44 x 10 ⁻²	1.94 x 10 ⁻³	1.78 x 10 ⁻⁴	6.52 x 10 ⁻⁶	271	225
LM118	B	1.22 × 10 ⁻¹	2.69 x 10 ⁻⁵	<u> </u>	-	30	175
LM111	В	7.77 x 10 ⁻³	3.93 x 10 ⁻³	\triangle	<u>-</u>	•	-
	D	2.14 x 10 ⁻³	1.35 x 10 ⁻³	1.89 x 10 ⁻³	1.73 x 10 ⁻³	201	250

NOTES:

SINGLE LOGNORMAL DISTRIBUTION, ADDITIONAL BURN-IN NOT RECOMMENDED.

ANSWERS LOSS OF THE PROPERTY OF THE PROPER

9.0 CONCLUSIONS

The results of this study indicate that linear microcircuit manufacturers have the capability of producing high reliability devices which would be acceptable for use in military applications. Also the MiL-M-38510 specification for testing the linear devices studied in this program appear adequate to fully electrically characterize the devices. However, there were differences between the same device type from different manufacturers and between different device types from the same manufacturer. These differences indicate that tighter controls over both the electrical testing and the manufacturing processes are necessar to produce high reliability devices.

Although the devices were procured as capable of meeting the MIL-M-38510 specifications, several of the devices failed to conform to all of the test specification limits. Initial electrical failures were a minimum in the one JAN qualified device, but were numerous in all other devices. In most cases the parameter end-point limits were expanded to obtain a sufficient number of devices for further evaluations. With the expanded limits, as many as 33% of a particular manufacturer's devices failed initial electrical tests. Although many parameter end-point limits had to be expanded, the MIL-M-38510 electrical test limits are adequate with the exception of the LM111 device. Each manufacturer's device failed different electrical parameters, and not all devices from a particular manufacturer failed a specific electrical parameter, indicating that the MIL-M-38510 electrical test limits were capable of being met.

Information obtained in testing the LM111 devices indicate the current MIL-M-38510/10304 (8 March 1977) is in need of revision. With the LM111 devices, the static and dynamic test circuit was impossible to stabilize. Several attempts to construct the MIL-M-38510 test circuit resulted in severe oscillations in the device under test. Attempts to reduce these oscillations for a particular parameter test only produced worse conditions for other parameters. The devices were eventually tested with two separate test fixtures, each of which was specially designed to dampen oscillations for specific parameters without affecting other test results. Due to oscillations, several tests were not performed with either fixture, including all

tests required at -55°C. It was beyond the scope of this program to further investigate the oscillating LMIIIs because the oscillations may have been partly or entirely the fault of the particular devices available at the time of procurement.

Revisions are necessary to some of the MIL-M-38510 specifications due to the nonlinearities of the gain of the operational amplifiers and the comparators, and the instability of the comparators. Linearity in the gain measurements can be increased by reducing the load current during the gain tests. It is further recommended that the emitter gain tests for the comparators be deleted due to the instability of the part in this configuration. Minor revisions to the specifications should also be made as detailed in section 5.4. With the above exceptions, all remaining MIL-M-38510 specifications/ methods are adequate to electrically characterize the devices evaluated in this report.

Maximum temperatures at which the linear microcircuits would operate satisfactorily during accelerated life tests were widely dispersed for the devices evaluated. Particular maximum temperatures varied for device types within the same family (LM108A and LM118) and also varied for different devices fabricated by the same manufacturer. A maximum temperature of 175°C was utilized for the LM118 devices, while a 250°C maximum was utilized for the LM109 and LM111 devices. During life tests, the output voltages of several device types were different from the voltage levels which would be present had the devices operated in the ~55°C to +125°C temperature range. Devices were either thermally biased (LM108A and LM111) or the outputs were suppressed by thermal protection networks within the die (LM109). It is believed that thermally biasing operational amplifiers and suppressing the output voltages of the regulators represent valid accelerated life test conditions. Therefore, the temperature at which thermal runaway occurs should be considered the limiting factor in selecting life test temperatures, not the temperature at which thermal biasing or voltage suppression occurs.

In procuring sufficient good devices from a single manufacturer some devices which failed initial electrical tests were returned for replacements.

Date codes on the replacement devices were different from the date codes on the original devices indicating the devices were from different lots. Although subsequent construction analysis noted no differences, the replacement devices exhibited parameter failures different from the failures of the initial devices. Lot to lot variations in linear devices were not determined in this contract due to limited sample sizes, but these variations should be considered in reliability evaluations.

The failure rates for the operational amplifiers (LM108A and Manufacturer B's LM118) ranged from 1.22 x 10^{-1} failures per hour to 8.02 x 10^{-5} failures per hour. The failure rates for the comparators (LM111) were in the 1 x 10^{-3} failure per hour range. The failure rates indicate that these particular devices would not be acceptable for most military applications. Also, additional burn-in would not reduce the failure rate for these devices. The voltage regulators (LM109 and 723) and Manufacturer C's LM118 operational amplifiers exhibited too few failures during the 4000 hour life tests to compute failure rates, but it is expected that these devices would have median lives greater than 4000 hours when operated at life test temperatures, and could be expected to exhibit acceptable failure rates for military applications.

The primary failure mechanisms for the LM108A operational amplifiers, Manufacturer B's LM118 operational amplifier, and the LM111 comparators were surface related. As a group, surface related failure mechanisms accounted for 76% of the total number of failures. Although, in many cases, the absolute cause of the failure could not be positively determined, those failures which are due to surface related mechanisms can be greatly reduced by tightening process controls.

10.0 REFERENCES

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- [9] I. Bazovsky, "Reliability Theory and Practice", Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1961.
- [10] L. R. Goldthwaite, "Failure Rate Study for the Log Normal Lifetime Model", IRE (NSRQCE) Conference, pp. 208-213, 1961.

APPENDIX A CONSTRUCTION ANALYSIS

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M385 1 0/10107	MANUFACTURER	C			,						•	•			•	•		A34
M38510/10201	MANUFACTURER	Q								•				,			٠	A46
M38510/10201	MANUFACTURER	C				•						•						A54
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CONSTRUCTION ANALYSIS

M38510/10104BGC

MANUFACTURER A

OPERATIONAL AMPLIFIER

DATE CODE 7543

MIUROCIRCUIT CONSTRUCTION INFORMATION

S/N: 11

DATE CODE: 7643

DATE: 5/9/77

PART MAME: Operational Amplifier MAMUMAGTURER'S PART NO.: 108A883B

MANUFACTURER: A

GENERIC PART NO.: LMIOBA

PACKAGE TYPE: 8 Pin Can

MILITARY SPECIFICATION 40.: M38510/10104860

A. PACKAGE DETAILS (Sen Figure A)-1)

Lead Material: Gold Plated Kovar Lead Finish - Internal: Gold Plate

- External: Gold Plate

- Feed Through: None

Header Haterial: Gold Plated Kovar Cap Material: Gold Plated Nickel

Case Seal Method: Weld

Lead Seal Material/Method: Matched Glass

B. INTERCONNECTION DETAILS (See Figure 91-2)

Die Mounting Macarial: Gold-Silicon Estectic

Interconnect Wire Material: Aluminum

Interconnect Wire Diameter: 0.0012 inch

Longest Interconnect Wire Langth: 0.086 inch

Wire Bond Type(s) Post: Ultrasonic (See Figure Al-4)

Die: Ultrasonic (See Figure A1-3)

C. DIE DETAILS (See Figure A1-6)

Passivation Type: Silicon Dioxide

Glassivation Type. Vapor Deposited Glass Basic Die Construction: Epitaxial Planar

Die Dimensions: 0.055 inch x 0.041 inch

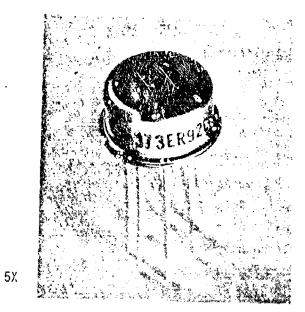
Metalization Type: Aluminum

Metalization Thickness: 13,748A

Scribe hethod: Mechanical

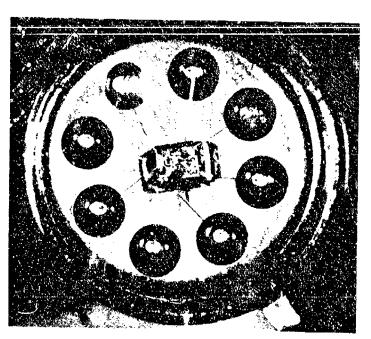
Bond Pad Size: 0.007 inch x 0.007 inch

 v_{CC} Stripe Cross-Sectional Area: 1 37 x 10^{-4} cm x 4.65 x 10^{-3} cm = 6.39 x 10^{-7} cm²



S/N11

FIGURE A1-1 - PACKAGE PHOTOGRAPH



10X

S/N11

FIGURE A1-2 - INTERCONNECT PHOTOGRAPH



530X SEM (SEM-1.2KV)

S/N11

FIGURE A1-3 - WIRE BOND AT DIE



530X SEM (SEM-1.2KV)

S/N11

FIGURE A1-4 - WIRL BOND AT POST

D. ELECTRICAL SCHEMATIC

Since the schematic for Manufacturer A was not included in military specification MIL-M-38510/10104, a schematic diagram was obtained from Manufacturer A. The accuracy of this schematic was confirmed by a detailed microscope examination of the die after glassivation removal. The schematic was found to be correct. The schematic is included as Figure A1-5 and the die photograph with circuit elements identified is included as Figure A1-5.

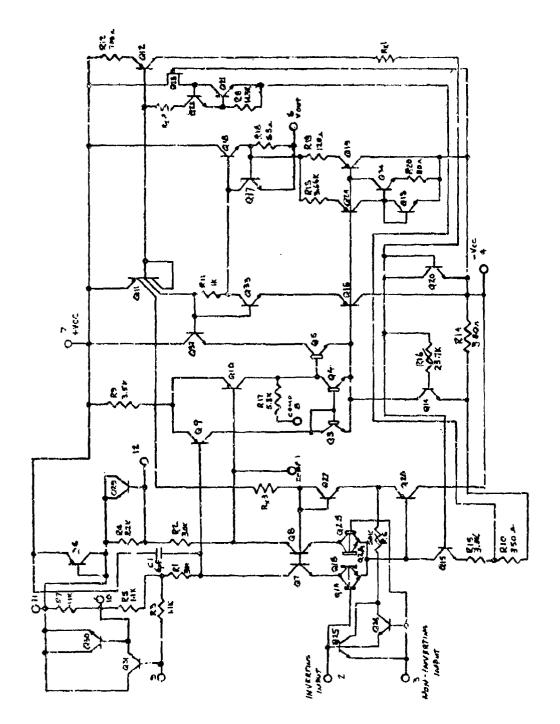
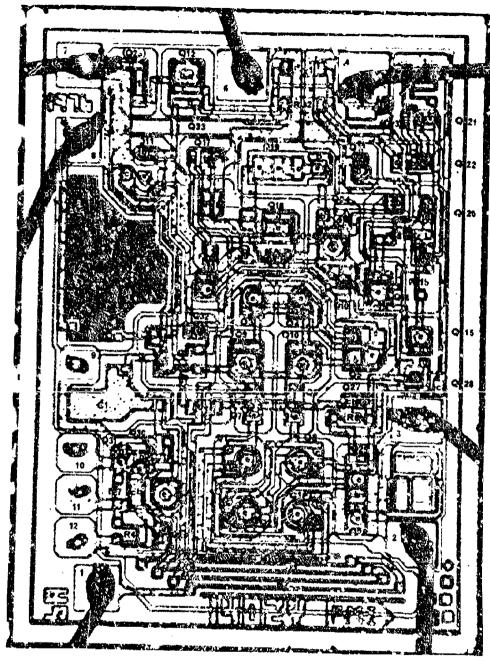


FIGURE A1-5 - SCHEMATIC DIAGRAM



134X S/N11

FIGURE A1-6 - DIE PHOTOGRAPH

E. COMPONENT DESCRIPTION

An examination of the die surface was conducted in order to determine the structure of each circuit element.

1. TRANSISTORS (Transistors listed together share a common N type collector or base tub.)

Vertical NPN	Vertical PNP	Lateral PNP	N Channel J FET
ણ ⊛	Q16	Q6 *	Q23
Q2 🕲	Q19	Q9	
Q3 * ҈	028	Q10	
Q4 🤁		Qll	
ე5 🥸		· Q12	
Q7		Q24	
Ú8		Q28	
Q13*			
Q14, Q34			•
Ų15			
Q17			
Ó18			
Q20 *			
Q21			
Q22			
Q25, Q26			
Q27 *			
Q29*, Q30*, Q31			
Q32 Q33			

^{*} Diode connected transistor.

 $[\]ensuremath{\mathfrak{G}}$ Super beta transistor.

2. RESISTORS

<u>P lype</u>	Squeezed P Type	N+ Crossunders				
R1 thru R5	R6	R _x l thru R _x 3				
R7 thru R15	Rio					
R17 thru R20						

CAPACITORS

MOS Thin Oxide Over N+

Cl

The schematic supplied by the manufacturer and the die itself contained a number of circuit elements and bonding pads not connected in this device. These are used to trim offset voltage by selectively zapping the transistors Q29, Q30 or Q31. Shorting CYP removes R4 from the circuit, shorting Q30 removes R7 and shorting Q31 removes C3 and R5 from the circuit. In the particular part being evaluated, transistor Q30 had been zapped (see Figure A1-7) removing R7 from the circuit.

An attempt was made to examine in detail the construction of the super-beta transistors Q1, Q2, Q3, Q4, and Q5. Several devices were angle sectioned and stained in an attempt to delineate the junctions. However all attempts failed to define the base, as shown in Figure A1-8. A discussion with the manufacturer revealed that the base is very near intrinsic and extremely difficult to show. They stated it could be done with limited success using diffraction in a scanning electron microscope. This is beyond the scope of this investigation and was not attempted.

F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-S1D-883, Method 2016.3.

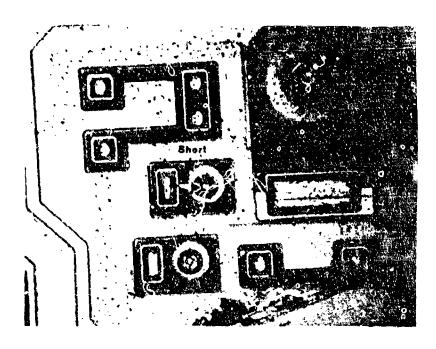


FIGURE A1-7 - TRANSISTOR Q31 WITH EMITTER BASE SHORT (MLTALIZATION REMOVED)



FIGURE A1-8 - CROSS SECTION OF A TYPICAL SUPER BETA TRANSISTOR

CONSTRUCTION ANALYSIS

M38510/10104BGC

MANUFACTURER B

OPERATIONAL AMPLIFIER

DATE CODE 7608

MICROCIACUIT CONSTRUCTION INFORMATION

S/N: 45 DATE CODE: 7608 DATE: 5/9/77

PART NAME: Operational Amplifier

MANUFACTURER'S PART NO.: LM108AH/10104BGC MANUFACTURER: B

GENERIC PART NO.: LM108A PACKAGE TYPE: 8 Pin Can

MILITARY SPECIFICATION NO.: M38510/10104BGC

A. PACKAGE DETAILS (See Figure A2-1)

Lead Material: Kcvar

Lead Finish - Internal: Gold Plate

- External: Gold Plate

· Feed Through: None

Header Material: Gold Plated Kovar

Cap Material: Nickel
Case Seal Method: Weld

Lead Seal Material/Method: Malched Glass

B. INTERCONNECTION DETAILS (See Figure A2-2)

Die Mounting Material: Gold Silicon Eutectic

Interconnect Wire Material: Aluminum
Interconnect Wire Diameter: 0.001 inch

Longest Interconnect Wire Length: 0.101 inch

Wire Bond Type(s) Post: Ultrasonic (See Figure A2-4)

Die: Ultrasonic (See Figure A2-3)

C. DIE DETAILS (See Figure A2-7)

Passivation Type: Silicon Dioxide

Glassivation Type: Phosphorous Glass

Basic Die Construction: Epitaxial Planar

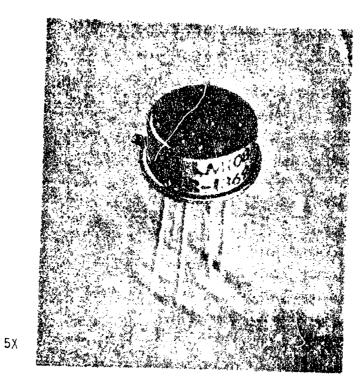
Die Dimensions: 0.058 inch x 0.057 inch

Metalization Type: Aluminum
Metalization Thickness: 22,913Å

Scribe Method: Mechanical

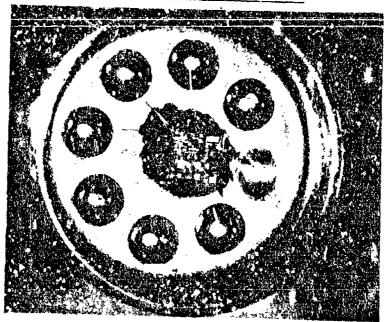
Bond Fad Size: 0.0047 inch x 0.0047 inch

 V_{CC} Suripe Cross-Sectional Area: 2.29 x 10^{-4} cm x 5.59 x 10^{-3} cm = 1.28 x 10^{-6} cm²



S/N45

FIGURE AZ-1 - PACKAGE PHOTOGRAPH



S/N45

FIGURE A2-2 - INTERCONNECTION PHOTOGRAPH

 $\chi_{\mathfrak{I}}$ r

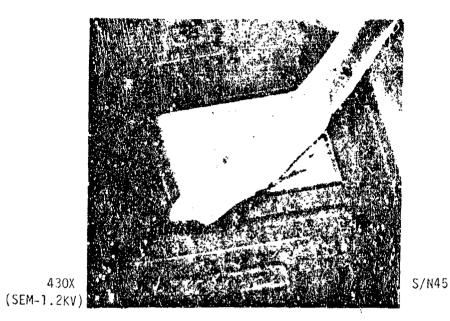


FIGURE A2-3 - WIRE BOND AT DIE



38UX (SEM-1.2 KV)

\$/N45

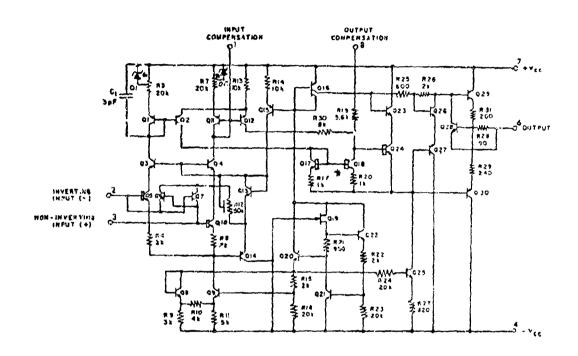
FIGURE A2-4 - WIRE BOND AT POST

D. ELECTRICAL SCHEMATIC

An electrical schematic of the device was prepared by modifying the schematic given in MIL-M-38510/10104 to conform to the actual circuitry on the die. The modification resulted from a microscopic examination of the die after removal of the glassivation and metalization. The corrected schematic is shown in Figure A2-5 and the die photomicrograph with components identified is Figure A2-6. The schematic modifications were as follows:

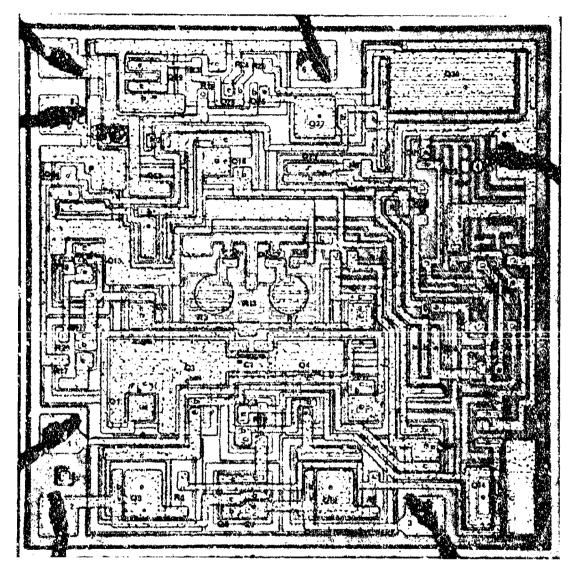
- The MIL-M-28510/10104 schematic included a resistor between the bases of Q17 and Q18 which is on the die but shorted by metalization and, therefore, not used.
- 2. Two zener diodes D1 and D2 added across a small portion of R3 and R7. The modifications are indicated on the schematic by an asterisk (*).

Resistors R3 and R7 and diodes D1 and D2 require additional explanation. These resistors have a small resistance path in series with the zener diodes. If the zener diodes are zapped a small reduction in the total resistance of either R3 or R7 will result. A discussion with the manufacturer revealed that at one time these were used to adjust offset. The manufacturer stated that they no longer find it necessary to adjust the device. The large circular pads over R3 and R7 were used to make contact during the diode zapping operation.



* Modifications to MIL-M-38510/10104 schematic.

FIGURE A2-5 - SCHEMATIC DIAGRAM



110X S/N45

FIGURE A2-6 - DIE PHOTOGRAPH

E. COMPONENT DESCRIPTION

The structure of each component was determined from examination of the die surface.

1. TRANSISTORS (Transistors listed together share a common N type collector or base tub.)

Vertical NPN	Vertical PNP	Lateral PNP	N Channel FET
Q3	Q14	()]*	୍ବୀ9
Q4	Q27	Q2	
Q5 €	Q30	Q11 *	
Q6 - Q7		Q12	
Q8*		Q15	
Q 9		Q16	
Q10 🏵			
Q13*			
Q17* 🏵			
⊕ 810			
Q 2 0			
Q21			
Q22			
Q23			
Q24 🏵			
Q25			
Q26, Q28			
Q29			

^{*} Diode connected transistors.

[★] Super beta transistors.

2. RESISTORS

Р Туре	Squeezed P Type	<u>N Epitaxial</u>
R3	R12	R21
R4	R24	
R7 thru R11		
R13 thru R17		
R19		
R20		
R22		
R23		
R25		
R26		

Reference designations R1, R2, R5, R6 and R18 are not used.

3. CAPACITORS

MOS plus PN junction

C1

Capacitor C1 is a metal oxide silicon capacitor with a parallel PN junction to increase capacitance. Figure A 2-7 illustrates the construction of this capacitor.

F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-STD-883, Method 2010.3.

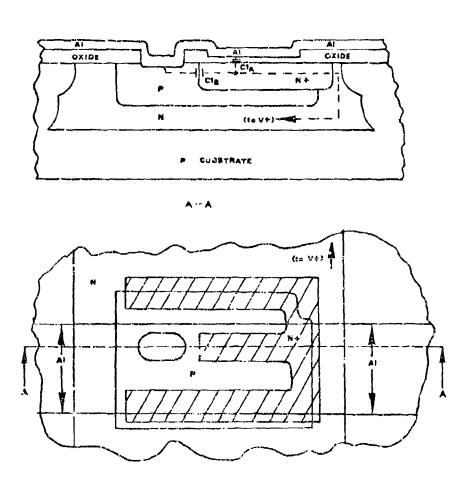


FIGURE A2-7 - CONSTRUCTION OF C1

CONSTRUCTION ANALYSIS

M38510/10107BGC

MANUFACTURER B

OPERATIONAL AMPLIFIER

DATE CODE 7632

MICROCIRCUIT CONSTRUCTION INFORMATION

S/N: 82 DATE CODE: 7632 PATE: 5/9/77

PART NAME: Operational Amplifier

MANUFACTURER'S PART NO.: LM118/10107BGC MANUFACTURER: 3

GENERIC PART NO.: LM118 PACKAGE TYPE: 3 Pin Can

MILITARY SPECIFICATION NO.: M38510/10107BGC

A. PACKAGE DETAILS (See Figure A3-1)

Lead Material: Kovar

Lead Finish - Internal: Gold Plate

- External: Gold Plate

- Feed Through: None

Header Material: Gold Plated Kovar

Cap Material: Nickel
Case Seal Method: Weld

Lead Seal Material/Method: Matched Glass

B. INTERCONNECTION DETAILS (See Figure A3-2)

Die Mounting Material: Gold Silicon Eutectic

Interconnect Wire Material: Aluminum
Interconnect Wire Diameter: 0.001 inch

Longest Interconnect Wire Length: 0.077 inch

Wire Bond Type(s) Post: Ultrasonic (See Figure A3-4)

Die: Ultrasonic (See Figure A3-3)

C. DIE DETAILS (See Figure A3-6)

Passivation Type: Silicon Dioxide Glassivation Type: Pnosphorus Glass

Basic Die Construction: Planar Epitaxial

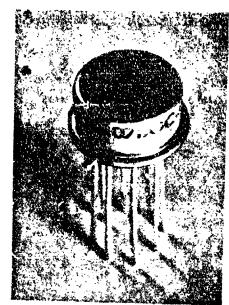
Die Dimensions: 0.075×0.050 inch

Metalization Type: Aluminum on Metalization Thickness: 10,160Å

Scribe Method: Mechanical

Bond Pad Size: 0.005 x 0.005 inch

 V_{CC} Stripe Cross Sectional Area: $1.02 \times 10^{-4} \text{cm} \times 2.67 \times 10^{-3} \text{cm} = 2.71 \times 10^{-7} \text{cm}^2$



S/N82

S/N82

FIGURE A3-1 - PACKAGE PHOTOGRAPH

5X

10X

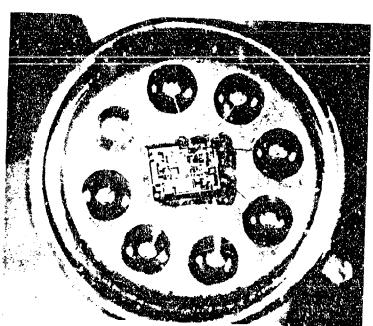


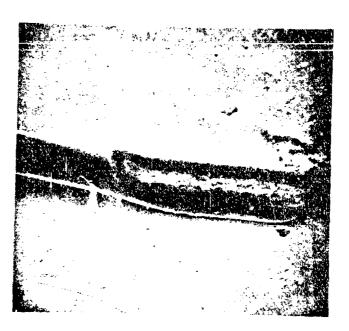
FIGURE A3-2 - INTERCONNECTION PHOTOGRAPH



360X (SEM-1.2KV)

S/N82

FIGURE A3-3- WIRE BOND AT DIE



440X (SEM-1.2KV)

S/N82

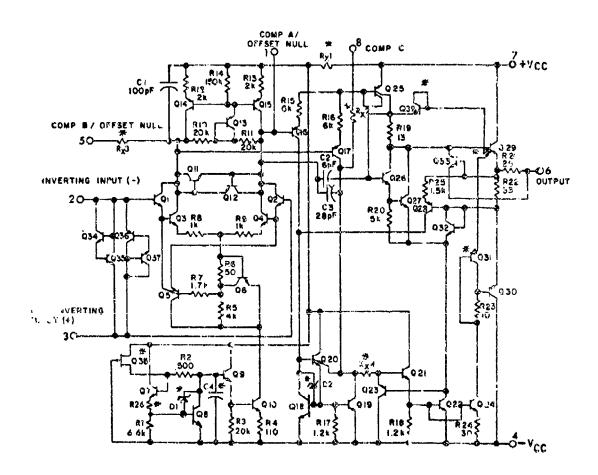
FIGURE A3-4 - WIRE BOND AT POST

D. ELECTRICAL SCHEMATIC

An electrical schematic of the device was prepared by modifying the schematic given in MIL-M-38510/10107 to conform to actual circuitry on the die. The modification resulted from a microscopic examination of the die with glassivation and metalization removed and from a metallurgical cross section. The corrected schematic is shown in Figure A3-5 and the components are identified in the die photograph shown in Figure A3-6. The schematic modifications consist of the following:

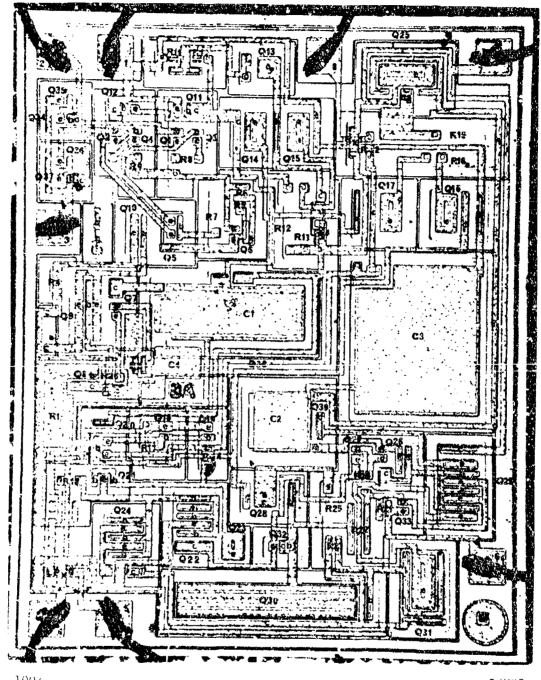
- 1) Added four diffused cross unders $(R_x 1 R_x 4)$
- 2) Addea resistor (R26)
- 3) Added a diode connected transistor (Q39)
- 4) Added collector-base clamp diodes to Q8 and Q18
- 5) Added a small value metal over substrate capacitor (C4)
- 6) Changed Q31 from NPN to PNP
- 7) Changed JFET reference designation to Q38 (to correct duplication of numbers)

The changes are indicated on the schematic with an asterisk (*).



* Additions or corrections to the MIL-M-38510/10107 schematic.

FIGURE A3-5 - COMPLETE ELECTRICAL SCHEMATIC



109X S/N32

FIGURE A3-6 - DIE PHOTOGRAPH AND COMPONENT IDENTIFICATION

E. COMPONENT DESCRIPTION

From examination of the die surrace and the cross sections, the structure of each component was determined.

1. TRANSISTORS (Transistors listed together share a common N-type collector or base tub.)

Vertical NFN	Vertical DNP	Lateral PNP	N Channel JFET
Q1, Q3, Q11*	Q23	Q13*	Q38
Q2, Q4, Q12*	Q30	Q14, Q15	
Q5, Q10		Q16	
QG		Q17	
Q7, Q9		Q25	
Q8		Q28	
Q18		Q31	
Q19			
Q20, Q21			
Q22			
Q24			
026, 027, 033			
Q29			
Q32*			
Q34*, Q35			
Q36, Q37*			
Q39*			

^{*} Diode connected transistor.

2. RESISTORS

P !ype	Squeezed P Type	N epitaxial	N [†] Crossunders
R1	Я5	R2, 3	R _x 1, 2, 3, 4
R4	R10, 11		^
26 thru 9	R14		
R12, 13	R20		
R15 thru 19			
R21 thru 26			

3. CAPACITORS

MOS (thin oxide over
$$N^+$$
)

MOS (thick oxide over substrate)

C2, 3

C4

C7

The structure of the four capacitors and transistors Q38 and Q39 require further discussion. Figure A3-7 is an etched metallurgical cross section of C1, C2 and Q38. The N channel junction field effect transistor Q38 is a squeezed N epitaxial resitor. The channel region is composed of N epitaxial silicon. The gate is composed of a P type base diffusion (upper channel boundary), a deep P type isolation diffusion (sidewall boundary) and the P type substrate lower boundary). The drain contact of the JFET is the N^{\dagger} diffusion of the R14 squeezed P type resistor and the source contact is the N^{\dagger} upper contact to R2.

Capacitors C2 and C3 are normal MOS N^{+} capacitors except that the N^{+} diffusion is preceded by a P type base diffusion. In C2, the P type diffusion is shorted to the N type tank via an N^{+} diffusion and the ohmic contact as shown in Figure A3-8(a). This contact is connected to an emitter of Q29 which results in a diode connected transistor Q39 being added to the schematic between Q29 and the N^{+} side of C2. The complete equivalent circuit for C2 is shown in Figure A3-8(b). In C3, all three diffusions, the N^{+} , the P type and the N tank are shorted together and, therefore, no additional circuit element exists.

C1 contains a P-N junction capacitor in parallel with a MOS capacitor to increase its capacitance as shown in Figure A3-S(a). The P-N capacitor is part of the MOS capacitor and uses a deep P^{\pm} isolation diffusion. The equivalent circuit of this capacitor is shown in Figure A3-9(b).

C4 is formed by expanding the metallization connected to the Q9 base/R2 contacts which adds additional capacitance between these points and the underlying substrate (V_{-}) .

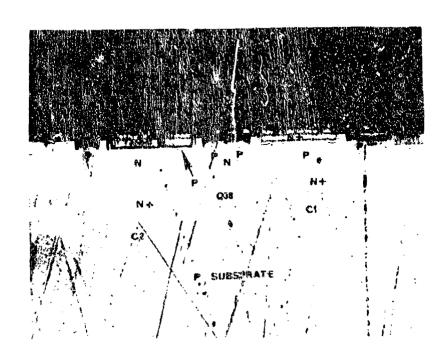
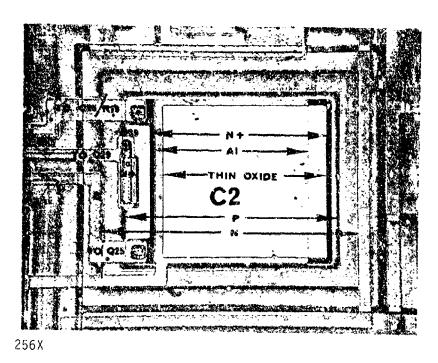


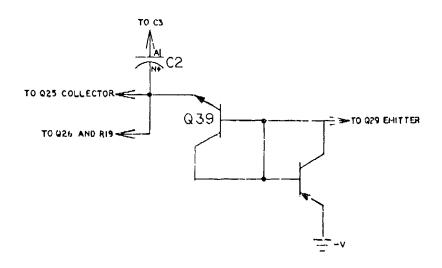
FIGURE A3-7 - METALLURGICAL CROSS SECTION (ETCHED) OF C2, Q38 AND C1

F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-STD-883, Method 2010.3.

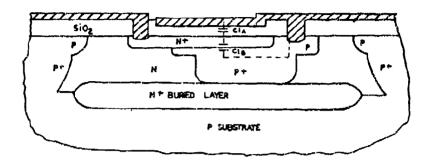


a) PHOTO OF C2 AFTER REMOVING THE METALLIZATION

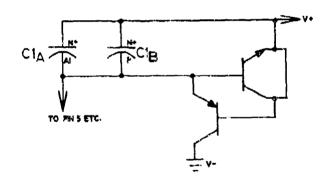


b) EQUIVALENT CIRCUIT OF C2

FIGURE A3-8 - PHOTOMICROGRAPH AND EQUIVALENT CIRCUIT OF C2



a) CROSS-SECTIONAL SKETCH OF CI



b) EQUIVALENT CIRCUIT OF CI

FIGURE A3-9 - DIFFUSION PROFILE AND EQUIVALENT CIRCUIT OF C1

CONSTRUCTION ANALYSIS

M38510/10107BGC

MANUFACTURER C

OPERATIONAL AMPLIFIER

DATE CODE 7651Q

MICROCIPCUIT CONSTRUCTION INFORMATION

S/N: 12 DATE CODE: 7651Q DATE: 5/9/77

PART NAME: Operational Amplifier

MAHUFACTURER'S PART NO.: M38510/10107BG MAHUFACTURER: C

GENERIC PART NO.: LMI18 PACKAGE TYPE: 8 Pin Can

MILITARY SPECIFICATION NO.: M38510/101078GC

A. PACKAGE DETAILS (See Figure A4-1)

Lead Material: Kovar

Lead Finish - Internal: Gold Plate

- External: Gold Plate

- Feed Through: None

Header Material: Gold Plated Kovar

Cap Material: Nickel
Case Seal Method: Weld

Lead Seal Material/Method: Matched Glass

B. INTERCONNECTION DETAILS (See Figure A4-2)

Die Mounting Material: Gold Silicon Eutectic

Interconnect Wire Material: Aluminum
Interconnect Wire Diameter: 0.0011 inch

Longest Interconnect Wire Length: 0.128 inch

Wire Bond Type(s) Post: Ultrasonic (See Figure A4-4)

Die: Ultrasonic (See Figure A4-3)

C. DIE DETAILS (See Figure A4-6)

Passivation Type: Silicon Dioxide

Glassivation Type: Phosphorus Glass

Basic Die Construction: Planar Epitaxial Die Dimensions: 0.084 inch x 0.077 inch

Metalization Type: Aluminum

Metalization Thickness: 49,988 A

Scribe Method: Mechanical

Bond Pad Size: 0.007 inch x 0.007 inch

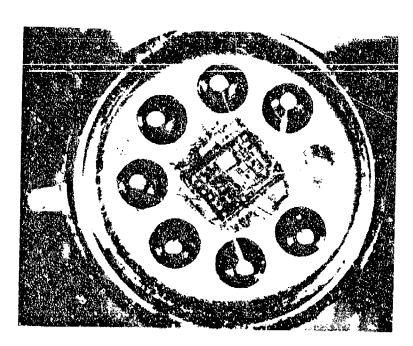
 $V_{\rm CC}$ Stripe Cross-Sectional Area: $4.50 \times 10^{-4} {\rm cm} \times 1.98 \times 10^{-3} {\rm cm} = 9.90 \times 10^{-7} {\rm cm}^2$



5X

S/N11

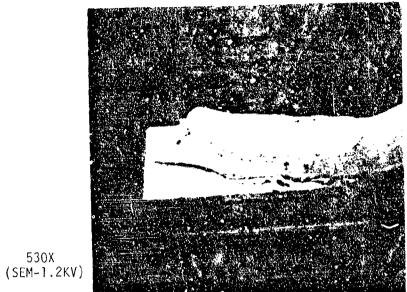
FIGURE A4-1 - PACKAGE PHOTOGRAPH



10X

S/N12

FIGURE A4-2 - INTERCONNECTION PHOTOGRAPH



S/N12

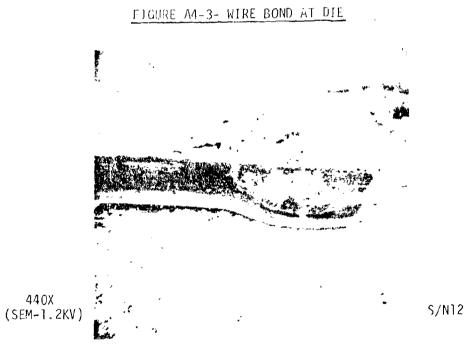


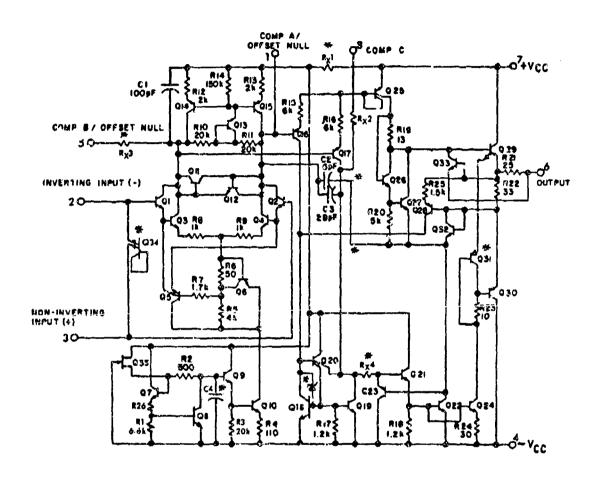
FIGURE A4-4 - WIRE BOND AT POST

D. ELECTRICAL SCHEMATIC

An electrical schematic of the device was prepared by modifying the schematic given in MIL-M-38510/10107 to conform to the actual circuitry on the die. The modification resulted from a microscopic examination of the die after glassivation removal and was aided by the previous study of the Manufacturer B device. The corrected schematic is shown in Figure A4-5 and the components are identified on the die photograph shown in Figure A4-6. The schematic modifications consist of the following.

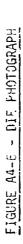
- a) Added four diffused crossovers ($\frac{1}{x}$ 1, $\frac{1}{x}$ 2, $\frac{1}{x}$ 3, $\frac{1}{x}$ 4)
- b) Added resistor (R26)
- c) Added a small value metal over substrate capacitor (C4)
- d) Changed Q31 from NPN to PNP
- e) Changed JFET reference designation to Q35 (duplication)
- f) Added collector-base clamp diode to Q18
- g) Changed input protection from 4 transistors to one dual emitter transistor
 (Q34)
- h) Removed connection between C2 and Q26 base, R19
- Added connection between C2 and R2O, Q27 emitter, Q32 emitter, Q22 collector, Q23 base

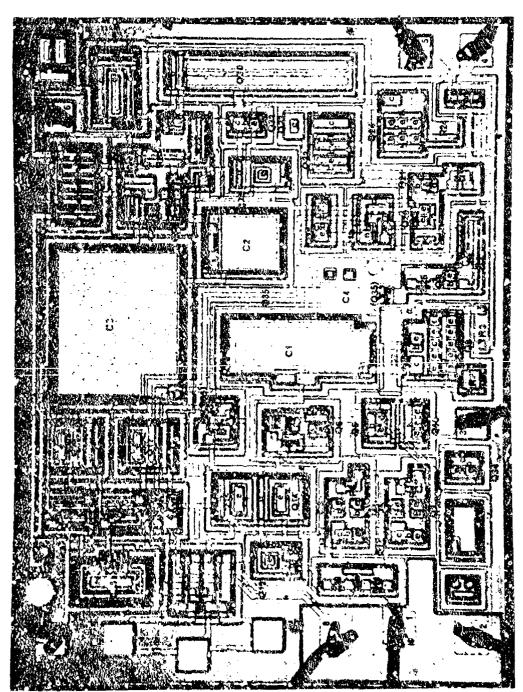
Changes are indicated in the schematic with an asterisk (*).



* Modifications to MIL-M-38510/10107 schematic.

FIGURE A4-5 - SCHEMATIC DIAGRAM





92 23 25

E. COMPONENT DESCRIPTION

From examination of the die surface and the similarity between this device and the Manufacturer B version, the structure of each component was determined.

1. TRANSISTORS (Transistors listed together share a common N-type collector or base tub.)

Vertical NPN	Vertical PNP	Lateral PNP	N Channel JFET
Q1, Q3, Q11*	Q23	Q13*	Q35
Q2, Q4, Q12*	Q3 0	Q14, Q15	
Q5, Q10		Q16	
Q6		017	
Q7, Q9		Q25	
Q8		Q28	
Q18		Q31	
Q19			
Q20, Q21		•	
Q22			
Q24			
Q26, Q27, Q33			
Q29			
Q32*·			
Q34.*			

^{*} Diode connected transistor.

2 RESISTORS

P Type	Squeezed P Type	N Epitaxial	H+ Crossunders
ลา	R5	R2	R _{3:} 1
R4 ·	R10	R3	R _x 2
R6 thru 9	R11		1,3
R12	R14		<u> </u>
R13	R20		χ.
R15 thru 19			
R21 thru 26			

CAPACITORS

MOS (thick oxide over N+)	MOS (thick oxide over substrate)	MOS + PN Junction
C2	C4	C1
C3		

The structure of the four capacitors and transistor Q35 require further discussion. The N-channel junction field effect transistor Q35 is a squeezed N-channel epitaxial resistor. The channel region is composed of N-epitaxial silicon. The gate is composed of a P-type base diffusion (upper channel boundary), a deep P-type isolation diffusion (sidewall boundary) and the P-type substrate (lower channel boundary). The drain contact of the JFET is the N+ diffusion of the R14 squeezed P-type resistor and the source contact is the N+ upper contact of R2. Refer to Figure A3-7 in Appendix A3 for a metallurgical cross section of the JFET since Q35 is constructed identically to Q38 in the Manufacturer B device.

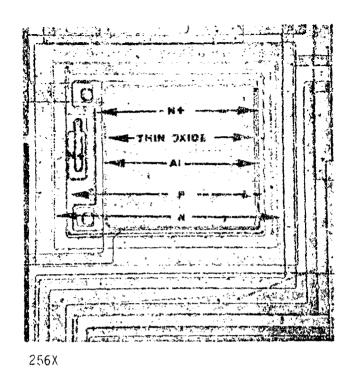
Capacitors C2 and C3 are also of the same construction as the same capacitors in the Manufacturer B device (Appendix A3). They are normal MOS N+ capacitors except the N+ diffusion is preceded by a P-type base diffusion. In C2 the P-type diffusion is shorted to the N-type tank via an N+ diffusion and the ohmic contact as shown in Figure A4-7(a). This contact is left unconnected in this device. The equivalent schematic of C2 is as shown in Figure A4-7(b). In C3 the three diffusions, the N+, the P type and the N tank are shorted together.

Cl contains a P-N capacitor in parallel with a MOS capacitor to increase its capacitance. As shown in Figure A4-8(a), the P-N capacitor is part of the MOS capacitor and uses a deep P+ isolation diffusion. The equivalent circuit of this capacitor is shown in Figure A4-8(b).

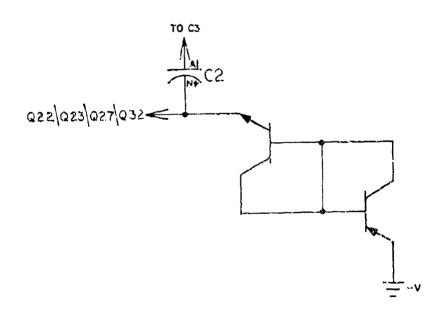
C4 is formed by expanding the metalization connected to the Q9 base/R2 contacts which add capacitance between these points and the underlying substrate (V-).

F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-STD-883, Method 2010.3.

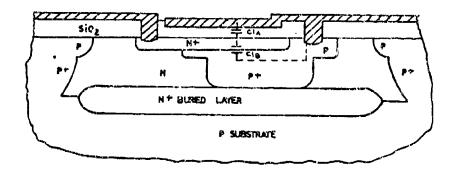


a) PHOTOMICROGRAPH OF C2 AFTER METALIZATION REMOVAL

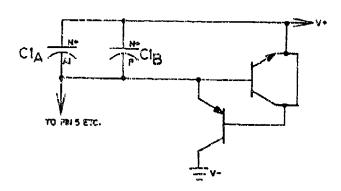


b) EQUIVALENT CIRCUIT OF C2

FIGURE A4-7 - PHOTOMICROGRAPH AND EQUIVALENT CIRCUIT OF CAPACITOR C2



a) CROSS-SECTIONAL SKETCH OF CI



b) EQUIVALENT CIRCUIT OF CI

FIGURE A4-8 - DIFFUSION PROFILE AND EQUIPMENT CIRCUIT OF CT

CONSTRUCTION ANALYSIS

M38510/10201BIC

MANUFACTURER D

PRECISION VOLTAGE REGULATOR

DATE CODE 7630

MICROCIRCUIT CONSTRUCTION INFORMATION

S/N: 51 DATE CODE: 7630 DATE: 7/8/77

PART NAME: Precision Voltage Regulator

MANUFACTURER'S PART NO.: M38510/10201BIC MANUFACTURER: D

GENERIC PART NO.: 723 PACKAGE TYPE: 10 Pin Can

MILITARY SPECIFICATION NO.: M38510/10201BIC

A. PACKAGE DETAILS (See Figure A5-1)

Lead Material: Kovar

Lead Finish - Internal: Gold Plate

- External: Gold Plate

- Feed Through: None

Header Material: Gold Plated Kovar

Cap Material: Nickel
Case Seal Method: Weld

Lead Seal Material/Method: Matched Glass

B. INTERCONNECTION DETAILS (See Figure A5-2)

Die Mounting Material: Gold-Silicon Eutectic

Interconnect Wire Material: Aluminum
Interconnect Wire Diameter: 0.001 inch

Longest Interconnect Wire Length: 0.105 inch

Wire Bond Type(s) Post: Ultrasonic (See Figure A5-4)

Die: Ultrasonic (See Figure A5-3)

C. DIE DETAILS (See Figure A5-6)

Passivation Type: Silicon Dioxide

Glassivation Type: Vapox

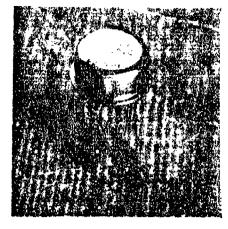
Basic Die Construction: Planar Epitaxial Die Dimensions: 0.057 inch x 0.048 inch

Metalization Type: Aluminum
Metalization Thickness: 22,811Å

Scribe Method: Mechanical

Bond Pad Size: 0.0044 inch x 0.0044 inch

 V_{CC} Stripe Cross-Sectional Area: 2.28 x 10^{-4} cm x 7.34 x 15^{-3} cm = 1.67 x 10^{-6} cm²



S/N51

FIGURE A5-1 - PACKAGE PHOTOGRAPH

3X

10X

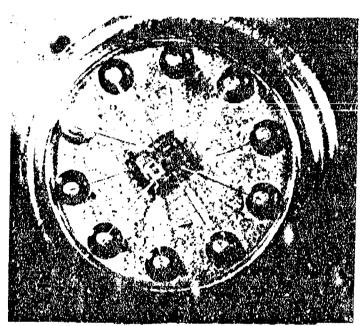
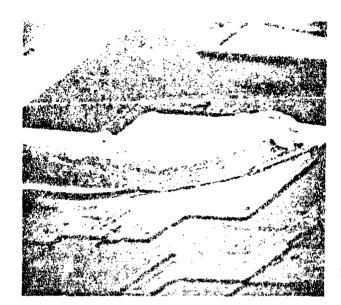


FIGURE A5-2 - INTERCONNECTION PHOTOGRAPH



700X (SEM~1.2KV)

S/N51

FIGURE A5-3 - WIRE BOND AT DIE



380X (SEM-1.2KV)

FIGURE A5-4 - WIRL BOND AT POST

D. ELECTRICAL SCHEMATIC

An electrical schematic of the device was obtained from MIL-M-38510/'0201 (Circuit C) and compared with the actual die configuration. The die layout agreed with the military specification schematic except for one area. Transistor Q14 shown in the schematic as a single emitter transistor actually has two emitters tied together and transistor Q18 is not connected in this device. The corrected schematic diagram is included as Figure A5-5 and a die photomicrograph with circuit elements identified is included as Figure A5-6.

E. COMPONENT DESCRIPTION

From examination of the die surface, the structure of each component was determined.

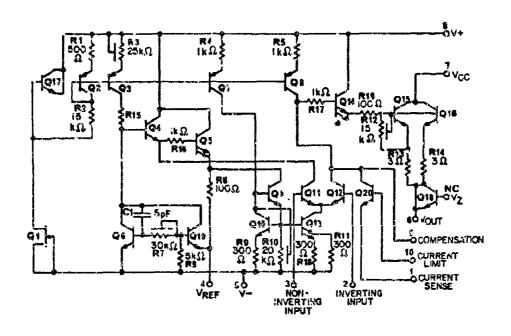
1. TRANSISTORS (Transistors listed together share a common N-type collector or base tub.)

Vertical NPN	Lateral PNP	N Channel JET
Q4, Q5, Q14, Q17*	Q2*, Q3, Q7 Q8	Q1
Q6, Q19		
Q9		
Q10		
Q11		
Q12, Q20		
Q13		
Q15, Q16		
Q18		

^{*} Diode connected transistors.

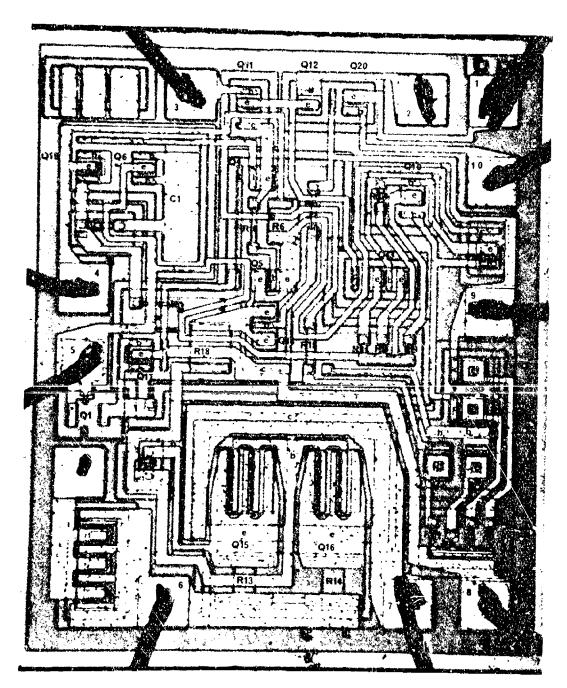
2. RESISTORS

<u>P Type</u>	Squeezed P Type	N-t
R1, R2	R3	R13
R4 thru R6	K7	R14
R8, R9	R10	
R11	R12	
R15 thru R18		



* Modifications to MJL-M-38510/10201 schematic.

FIGURE A5-5 - ELECTRICAL SCHEMATIC DIAGRAM



127% S/N51

FIGURE A5-6 - DIE PHOTOGRAPH

3. CAPACITORS

MCS (thin oxide over N+)

C1

F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-STD-883, Method 2010.3.

CONSTRUCTION ANALYSIS

M38510/10201BIC

MANUFACTURER C

PRECISION VOLTAGE REGULATOR

DATE CODE 7649P

MICROCIRCUIT CONSTRUCTION INFORMATION

S/N: 51

DATE CODE: 7649P

DATE: 2/8/77

PART NAME: Precision Voltage Regulator

MANUFACTURER'S PART NO .: 723HMB

MANUFACTURER: C

GENERIC PART NO.: 7°3

PACKAGE TYPE: 10 Pin Can

MILITARY SPECIFICATION NO.: M38510/10201EIC

A. PACKAGE DETAILS (See Figure A6-1)

Lead Material: Kovar

Lead Finish - Internal: Gold Plate

- External: Gold Plate

- Feed Through: None

Header Material: Gold Plated Kovar

Cap Material: Nickel Case Seal Method: Weld

Lead Seal Material/Method: Matched Glass

B. INTERCONNECTION DETAILS (See Figure A6-2)

Die Mounting Material: Gold Silicon Eutectic

Interconnect Wire Material: Aluminum Interconnect Wire Diameter: 0.0012 inch

Longest Interconnect Wire Length: 0.162 inch

Wire Bond Type(s) Post: Ultrasonic (See Figure A6-4)

Dia: Ultrasonic (See Figure A6-3)

C. DIE DETAILS (See Figure A6-6)

Passivation Type: Silicon Dioxide

Glassivation Type: Silox

Basic Die Construction: Planar

Die Dimensions: 0.037 inch x 0.049 inch

Metalization Type: Aluminum

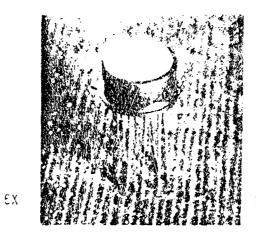
Metalization Thickness: 19.522A

Scribe Method: Mechanical

Bond Pad Size: 0.004 incl. x 0.004 inch.

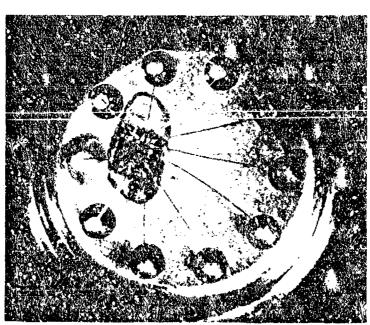
 V_{CC} Scribe Cross-Sectional Area: 1.96 x 10^{-4} cm x 2.26 x 10^{-2} cm = 4.42 x 10^{-5} cm²

A55



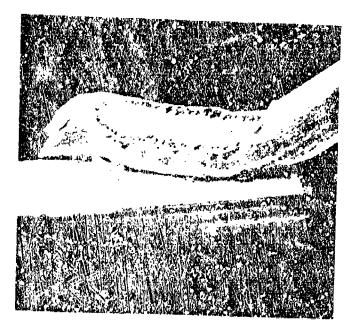
S/N51

FIGURE A6-1 - PACKAGE PHOTOGRAPH



10x

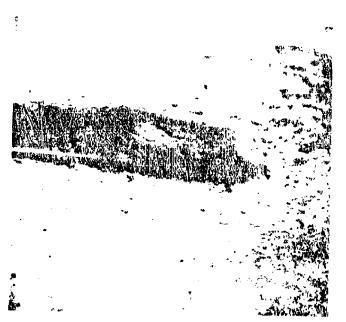
FIGURE AG-2 - INTERCONNECTION PHOTOGRAPH



520X (VMS.1.2MBP)

\$/1157

FIGURE AG-0 - WIRL BOND AT DIE



430X (SEM-1.2KV)

FIGURE A6-4 - WIRL POND AT POST

D. COMPONENT DESCRIPTION

Since a schematic for Manufacturer C device is not included in MIL-M-38510/10201, the closest equivalent was selected (Circuit C) and this schematic was modified to agree with the actual circuit determined from a microscopic examination of the die. The actual schematic is included as Figure A6-5 and the die photograph with circuit elements identified is included as Figure A6-6. The following modification was made:

1. The resistor between Q3 collector and Q4 base does not exist and was removed from the schematic.

The change is indicated on the schematic by an asterisk (*).

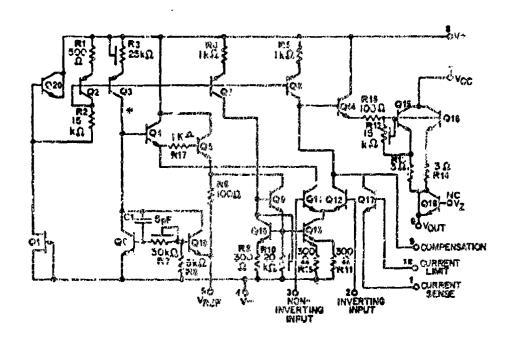
E. COMPONENT DESCRIPTION

from examination of the die surface, the structure of each component was determined.

1. TRANSISTORS (Transistors listed together share a common N-type collector or base tub.)

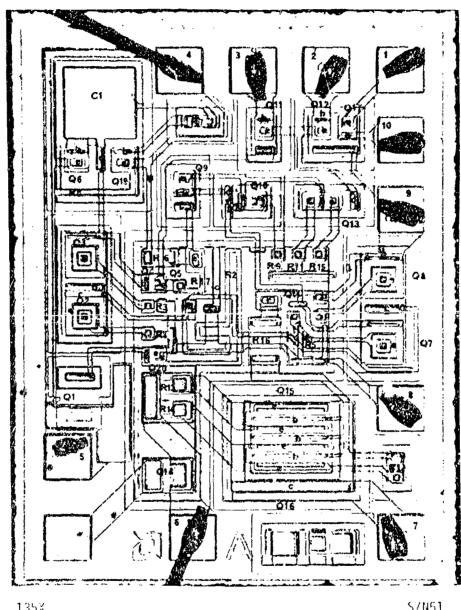
Vertical NPN Lateral PNP	N Channel JFET
Q4, Q5, Q14, Q20*	٠Į٦
Q6, Q19	
Q9	
Q10	
011	
Q12, Q17	
Q13	
Q15, 916	
QI8*	

* Diode connected transistor.



* Modifications to MIL-M-38510/10201 schematic.

FIGURE A6-5 - ELECTRICAL SCHEMATIC DIAGRAM



S/N51 135X

FIGURE A6-6 - DIE PHOTOGRAPH

2. RESISTORS

P Type

Squeezed P Type

 N^+

R1, R2

R3, R7, R10, R12

R13, R14

R4 thru R6

R8, R9

R11

R15 thru R17

3. CAPACITORS

MOS (thin oxide over N⁺)

C1

F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-STD-883, Method 2010.3.

CONSTRUCTION ANALYSIS

M38510/10701BXC

MANUFACTURER D

VOLTAGE REGULATOR

DATE CODE 7432

MICROCIRCUIT CONSTRUCTION INFORMATION

S/N:

105

DATE CODE:

7432

DATE:

5/9/77

PART NAME:

VOLTAGE REGULATOR

MANUFACTURERS PART NO.

F78M05HM0B

MANUFACTURER:

GENERIC PART NO:

78M05

PACKAGE TYPE:

T0-5

MILITARY SPECIFICATION NO:

M38510/10701BXC

PACKAGE DETAILS (See Figure A7-1)

Lead Material:

Kovar

Lead Finish - Internal:

Golo Plate

- External:

Gold Plate

- Feed Through: None

Header Material:

Gold Plated Kovar

Cap Material:

Nickel

Case Seal Method:

Weld

Lead Seal Material/Method: Matched Glass

INTERCONNECTIONS DETAILS (See Figure A7-2)

Die Mounting Material:

Gold Silicon Eutectic

Interconnect Wire Material: Aluminum

Interconnect Wire Diameter: 0.002 inch

Longest Interconnect Wire Length: 0.097 inch

Die:

Wire Bond Type (s) Post: Ultrasonic (See Figure A7-4) Ultrasonic (Sec Figure A7-3)

DIE DETAILS (See Figure A7-6) ۲.

Passivation Type: Glassivation Type:

Basic Die Construction:

Die Dimensions:

Metalization Type: Metalization Thickness: Scribe Method:

Silicon Dioxide

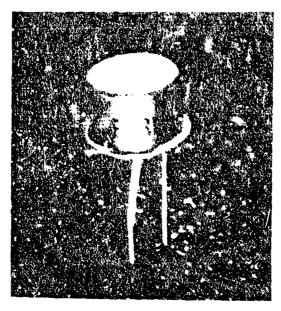
Vapox

Planar Epitaxial

0.074 inch x 0.069 inch

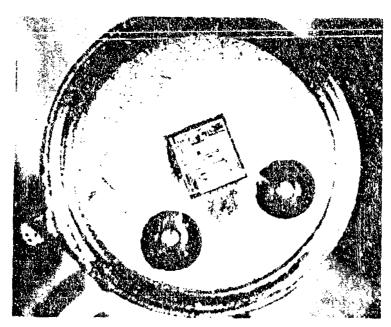
Aluminum 12,988Å Mechanical

Bond Pad Size: 0.0066 inch x 0.0068 inch
Vcc Stripe Cross-Sectional Area: 1.30x10-4cmx1.35x10-2cmx1.76x10-6cm2



S/N104

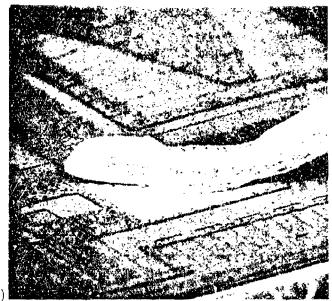
FIGURE A7-1- PACKAGE PHOTOGRAPH



S/N104

FIGURE A7-2- INTERCONNECTION PHOTOGRAPH

10X



270X (SEM-1.2KV)

S/N105

FIGURE A7-3- WIRE BOND AT DIE

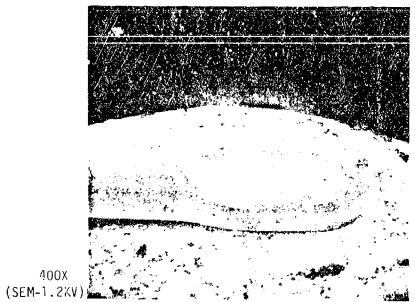


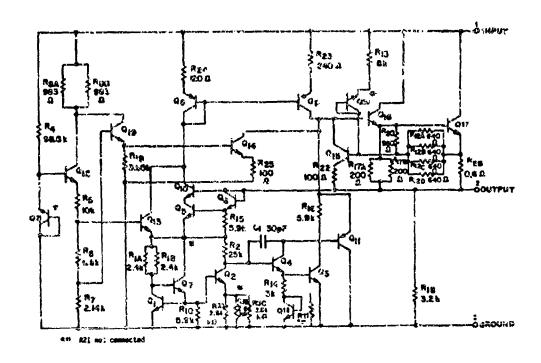
FIGURE A7-4- WIRE BOND AT POST

D. ELECTRICAL SCHEMATIC

An electrical schematic of the device was prepared by modifying the schematic in MIL-M-38510/107. Schematic "C" for device 02 was selected as being the closest match to the circuitry on the die. The corrected schematic is included as Figure A7-5 and the die photomicrograph with circuit elements identified is shown in Figure A7-6. The schemacic modifications consisted of the following:

- 1. Diodes D1 and D2 of the military specifications were changed to diode connected transistor Q20 and Q21.
- 2. Q5 emitter was connected to Q13 and the junction of R2 and R15.
- 3. R3 was changed to 3 parallel resistors.

The changes are indicated on the schematic diagram with an asterisk (*). In addition there are nine unconnected and undesignated resistors since this same die is used for a number of different voltages.



*MODIFICATIONS TO MIL-M-38510/10702 SCHEMATIC

FIGURE A7-5 - ELECTRICAL SCHEMATIC DIAGRAM

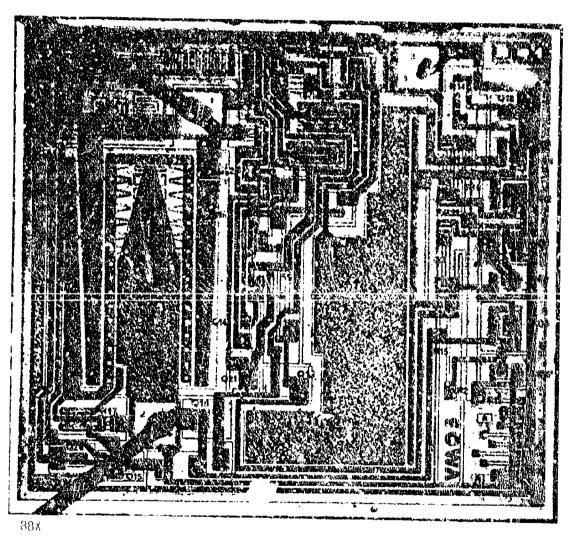


FIGURE A7-6 - DIE PHOTOGRAPH

E. COMPONENT DESCRIPTION

An examination of the die surface was conducted after removal of the glassivation and metallization in order to determine the structure of each circuit element.

1. TRANSISTORS (Transistors listed together share a common N type collector or base type diffusion)

<u>Vertical NFN</u>	Vertical PNP	Lateral PNP
Q1	Qll	Q8*, Q9
01 Q2 Q3, Q4		
Q5 Q6 *		
Q7 Q10		
Q12, Q19 Q13		
014 215		
016, Q17 Q18*		
Q20*		
Q21 *		

*dioda connected transistors

2. RESISTORS

P type

k! through R8

R10

K12 through R25

(Reference designations R9 and R11 are not used in the MIL-M-38510/10702 schematic C)

R_{EB}: The resistor designated R_{EB} represents a group of parallel emitter ballast resistors incorporated into the large power transistor Q17 to equalize the current di tribution over the full length of the transistor. A photomicrograph of a portion of transistor Q17 after removal of the glassivation and metalization is included as Figure A7-7. The extra base type diffusions around the emitter contacts create restricted current paths to the emitter contactor.

3. CAPACITORS

MOS (thick oxide over N)

Сı

F. QUALITY OF WORKMANSHIP

The quality of workmanuhip is considered acceptable per MIL-STO-883. Method 2010.3.

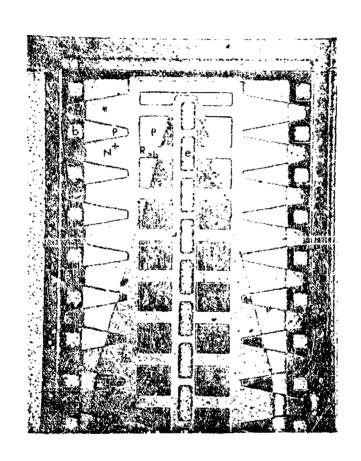


FIGURE 7-7 - TRANSISTOR Q17

CONSTRUCTION ANALYSIS

M38510/10701BXC

MANUFACTURER B

VOLTAGE REGULATOR

DATE CODE 7552

MICROCIRCUIT CONSTRUCTION INFORMATION

S/N:

43

DATE CODE: 7552

DATE:

5/9/77

PART NAME:

VOLTAGE REGULATOR

MANUFACTURERS PART NG:

LM109/10701/BXC

MANUFACTURER:

GENERIC PART NO:

LM109

PACKAGE TYPE:

TO-5

MILITARY SPECIFICATION NG: M38510/10701BXC

PACKAGE DETAILS (See Figure A8-1)

Lead Material:

Kovar

Lead Finish - Internal:

Gold Plate

- External: - Feed Through: Gold Plate None

Header Material: Cap Material:

Gold Plated Kovar

Case Seal Method:

Nickel | Reld

Lead Sea! Material/Method:

Matched Glass

INTERCONNECTION DETAILS (See Figure A8-2)

Die Mounting Material:

Gold - Silicon Eutectic

Interconnect Wire Material: Interconnect Wire Diameter:

Aluminum .0032 inch

Longest Interconnect Wire Length: 0.128 inch

Wire Bond Type (s) Post: Ultrasonic (See Figure A8-4)
Die: Ultrasonic (See Figure A8-3)

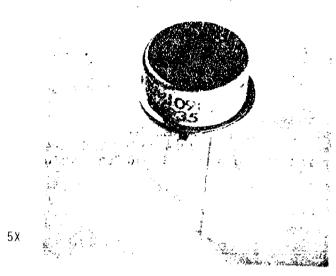
DIE DETAILS (See Figure A8-6) С.

Passivation Type: Glassivation Type: Basic Die Construction:

Die Dimensions:

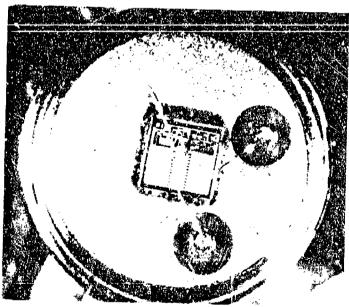
Metalization Type:
Metalization Thickness
Scribe Method:
Bond Pad Size:
Vcc Stripe Cross-Sectional Area: 1.10x10⁻⁴cmx1.34x10⁻²cm=1.47x10⁻⁶cm²

Silicon Dioxide Phosphorus Glass
Planar Epitaxial
0.084 inch x 0.077 inch



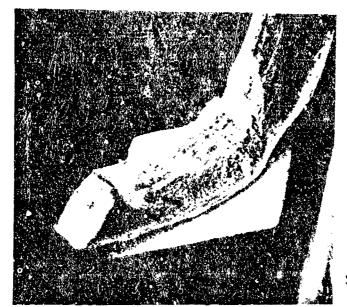
S/N42

FIGURE A8-1- PACKAGE PHOTOGRAPH



10X

FIGURE A8-2- INTERCONNECTION PHOTOGRAPH



300X (SEM-1.2KV)

S/N43

FIGURE A8-3 -- WIRE BOND AT DIE



250X (SEM-1.2KV)

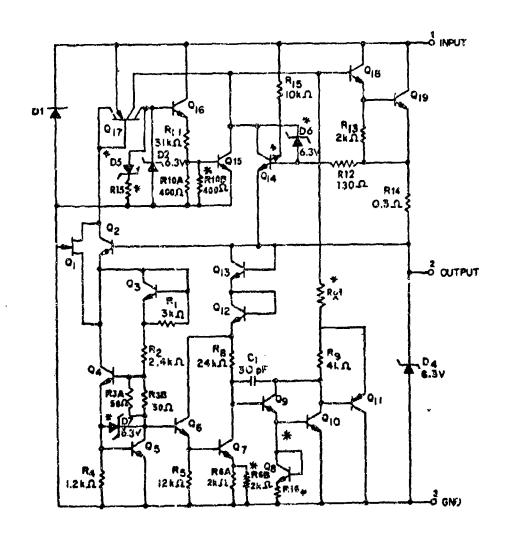
FIGURE A8-4- WIRE BOND AT POST

D. ELECTRICAL SCHEMATIC

An electrical schematic diagram was prepared by modifying the schematic included in MIL-M-38510/107 for device 01 to conform to the actual circuitry on the die. The modifications resulted from a detailed microscopic study of the die and included removal of the glassivation and metalization. The modified schematic is shown as Figure A8-5. A die photomicrograph with the circuit components identified is included as Figure A8-6. The schematic modifications were as follows:

- 1. Resistor R10 is two resistors in parallel.
- 2. Resistor R6 is two resistors in parallel.
- 3. Diode D3 of the MIL-M-38510 schematic was changed to an additional emitter on Q14.
- 4. Crossunder Rxl was added.
- 5. Resistor R16 was added between Q8 emitter and terminal 3.
- 6. Resistor R7 does not exist on the die.
- 7. Resistor R15 and diode D5 were added across D2.
- 8. Added D6 across the C-B junction of Q14.
- 9. Added D7 across the C-B junction of Q5.

The modifications are indicated on the schematic diagram with an asterisk (*).



*MODIFICATIONS TO MIL-M-38510/10701 SCHEMATIC

FIGURE A8-5 - ELECTRICAL SCHEMATIC DIAGRAM

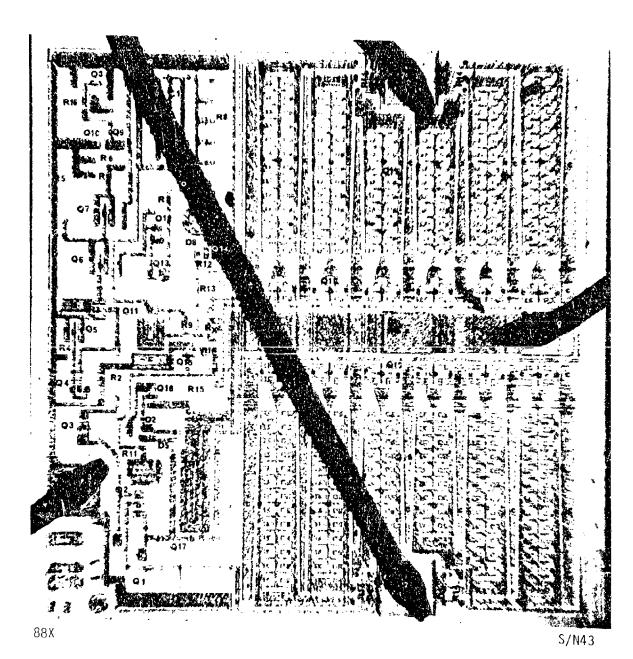


FIGURE A8-6 - DIE PHOTOGRAPH

E. COMPONENT DESCRIPTION

An examination of the die was conducted in order to determine the structure of each circuit element.

1. TRANSISTORS (Transistors listed together share a common N type collector or base tub)

<u>Vertical NPN</u>	Vertical PNP	Lateral PNP	N Channel J FET
Q2 Q3*, Q4 Q5 Q6 Q7 Q8* Q9, Q10 Q12* Q13* Q14, Q15 Q16 Q18 Q19	Q;1	Q1 <i>7</i>	Q1

*diode connected transistors

2. DIODES

PN D1	PN+
D1/*7	D2
	D4
	D5
	03
	D7

⚠Collector isolation diode of Q19

3. RESISTORS

P type	N±.	Squeezed P type
R1 thru R6	R14	R15
R8 thru R13	RxT	
R16		

Reference designation R7 removed

4. CAPACITOR

<u> Emilter - Base Junction Capacitor</u>

Cl

F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-STD-883, Method 2010.3.

CONSTRUCTION ANALYSIS

M38510/10304BGC

MANUFACTURER D

PRECISION VOLTAGE COMPARATOR/BUFFER

DATE CODE 7612

The second secon

MICROCIRCUIT CONSTRUCTION INFORMATION

311 S/N:

DATE CODE:

7612

DATE: 7/20/77

PART NAME:

PRECISION VOLTAGE COMPARATOR/BUFFER

MANUFACTURERS PART NO.

μA111HMQB

MANUFACTURER:

D

GENERIC PART NO:

LMIII

PACKAGE TYPE:

8 LEAD CAN

MILITARY SPECIFICATION NO:

M38510/10304BGC

A. PACKAGE DETAILS (See Figure A9-1)

Lead Material:

Kovar

Lead Finish - Internal:

Gold Plate

- External: - Feed Through: Cold Plate None

Header Material:

Gold Plated Kovar

Cap Material:

Nickel

Case Seal Method:

Weid

Lead Seal Material/Method:

Matched Gines

B. INTERCONNECTION DETAILS (See Figure AS-2)

Die Mounting Material:

Gold-Silicon Eutectic

Interconnect Wire Material:

Altered trace 0.0012 inch

Interconnect Wire Diameter: Longest Interconnect Wire Length: 0.102 tuch

Wire Bond Type (s) Post: Ultrasonic (See Figure AS-4)

Die:

Ultrasonic (See Figure A9-3)

ί. DIE DETAILS (See Figure A9-8)

Passivation Type: Glassivation Type: Silicon Dioxide Silicon Dioxide Planar Epitaxial 0.043 inch x 0.064 inch Basic Die Construction: Die Dimensions:

Mctalization Type: Aluminum 11,938Å Metalization Thickness: Scribe Method: Mechanical

Bond Pad Size: 0.004 inch x 0.004 inch ycc Stripe Cross-Sectional Area: 1.19x10-4cmx2.54x10-3cm=3.02x10-7cm²

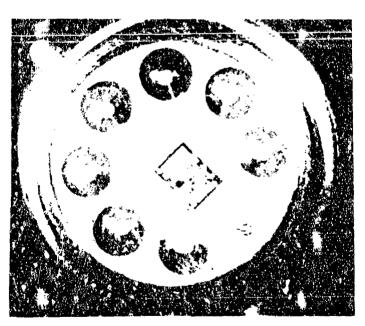


S/N 311

FIGURE A9-1 - PACKAGE PHOTOGRAPH

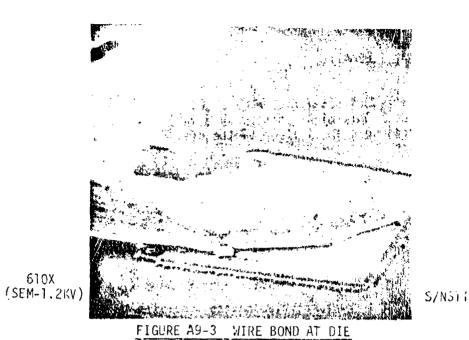
3X

10X



S/N 311

FIGURE A9-2 - INTERCONMECTION PHOTOGRAPH



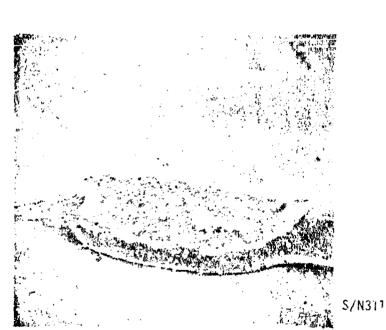


FIGURE AC-4-WIRE BOND AT POST

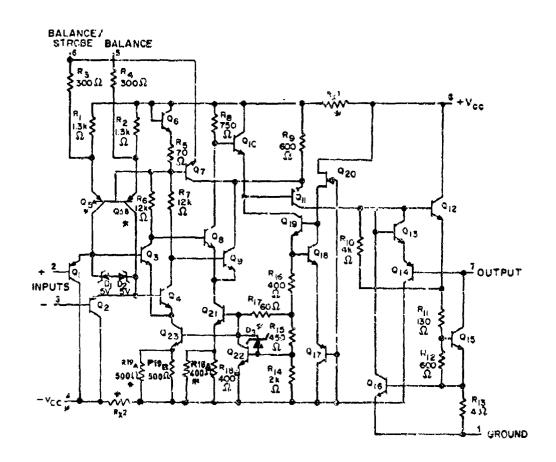
610X (SEM-1.2KV)

D. ELECTRICAL SCHEMATIC

The MIL-M-38510/10304 schematic "A" was determined to be the schematic for this device. Only minor changes were made to this schematic as a result of microscopic examination of the die. The schematic modifications are as follows:

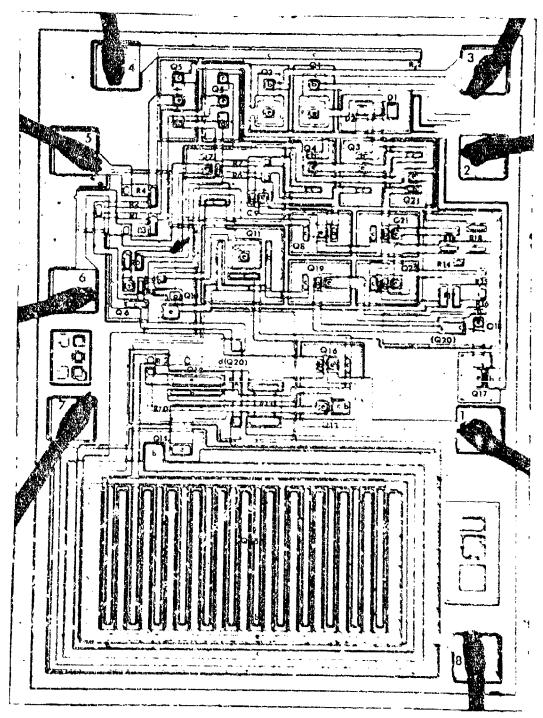
- 1. Q5 is actually two separate transistors, therefore one is designated Q5A and the other Q53.
- 2. Crossunders RxT and Rx2 were added.
- 3. R18 and R19 are actually two resistors in parallel.
- 4. D3 was added across the C-B junction of Q22.

These modifications are identified on the schematic diagram (Figure A9-5) by an asterisk (*). A die photomicrograph with the circuit elements identified is included as Figure A9-6.



*MODIFICATIONS TO MIL-M 38510/10304 SCHEMATIC

FIGURE A95 - ELECTRICAL SCHEMATIC DIAGRAM



130X

S/N 311

FIGURE A9-6 - DIE PHOTOGRAPH

E. COMPONENT DESCRIPTION

An examination of the die surface was conducted after removal of the glassivation and metallization in order to determine the structure of each circuit element.

1. TRANSISTORS (Transistors listed together share a common N type collector or base tub)

Vertical NPN	Vertical PNP	Lateral PNP	N Channel J FET
\$3 Q4 Q6*, Q10 Q7, Q9 Q8 Q12 Q13*, Q16 Q15 Q18 Q19 Q21 Q22 Q23	Q1 Q2 Q14 Q17*	Q5A Q5B Q11	Q20

*Diode connected transistors.

2. DIODES

D1 D2 D3

3. RESISTORS

<u>P typ</u> e	N+
R1 thru R12 R14 thru R19	R13 Rx1
	Rx2

F. QUALITY OF WORKMANSHIP

The quality of workmanship i considered acceptable per MIL-STD-883, Method 2010.3.

CONSTRUCTION ANALYSIS

M38510/10304BGC

MANUFACTURER B

PRECISION VOLTAGE COMPARATOR/BUFFER

DATE CODE 7601

MICROCIRCUIT CONSTRUCTION INFORMATION

\$/N: 311 DATE CODE:

7601

DATE:

7/20/77

PART NAME:

PRECISION VOLTAGE COMPARATOR/BUFFER

MANUFACTURERS PART NO.

LM111H/10304BGC

MANUFACTURER: B

GENERIC PAI NO.

LM111

PACKAGE TYPE

8 LEAD CAN

MILITARY SPECIFICATION NO:

M38510/10304BGC

Α. PACKAGE DETAILS (See Figure A10-1)

Lead Material:

Kovar

Lead Finish - Internal:

Gold Plate Gold Plate

- External:

None

- Feed Through:

Gold Plated Kovar

Header Material: Cap Material:

Nickel

Case Seal Method:

Weld

Lead Seal Material/Method:

Matched Glass

INTERCONNECTION DETAILS (See Figure A10-2) В.

Die Mounting Material:

Gold Silicon Eutectic

Interconnect Wire Material: Interconnect Wire Diameter: Aluminum. 0.0011 inch

Longest Interconnect Wire Length: 0.102 inch

Wire Bond Type (s) Post: Ultrasonic (See Figure A10-4)
Die: Ultrasonic (See Figure A10-3)

DIE DETAILS (See Figure A10-6)

Passivation Type: Glassivation Type: Basic Die Construction: Die Dimensions:

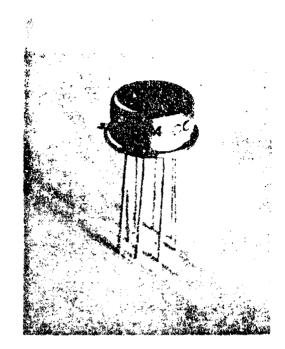
Metalization Type: Metalization Thickness: Scribe Method:

Silicon Dioxide Silicon Dioxide Planar Epitaxial

0.045 inch $\times 0.063$ inch

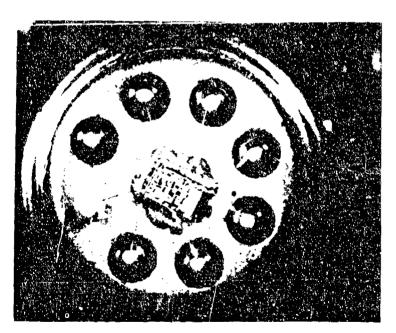
Aluminym 14.732Å Mechanical

Bond Pad Size: 0.0034 inch x 0.0034 inch Vcc Stripe Cross Sectiona! Area: 9.88x10⁻³cmx1.47x10⁻⁴cm=1.46x10⁻⁶cm²



S/N 311

FIGURE A10-1-PACKAGE PHOTOGRAPH

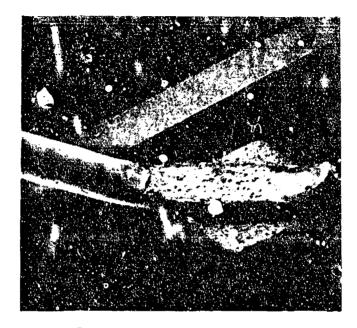


10x

3 X

S/N 311

FIGURE 10-2- INTERCONNECTION PHOTOGRAPH



450X (SEM-1.2KV)

S/N 311

S/N 311

FIGURE A-10 - WIRE BOND AT DIE



680X (SEM-1.2KV)

FIGURE A10-4-WIRE BOND AT POST

D. CLECTRICAL SCHEMATIC

The MIL-M-38510/10301 schematic "B" was determined to be the schematic for this device. A comparison between this schematic and the actual die layout was made after removal of glassivation and metalization. A number of changes in the schematic were required to produce agreement with the actual die layout.

- 1. Crossunders Rx1 and Rx2 were added.
- 2. Q5 is actually two separate transistors; therefore, one is designated Q5A and the other Q5B.
- 3. The diode shown connected to the collector of Q15 is actually a verticle PNP transistor (there is no buried layer under the emitter diffusion); therefore, the diode was changed to Q24.
- 4. Diode D5 was added across the C-B junction of Q22.

Changes in the schematic are indicated on the schematic diagram (Figure AlO-5) with an asterisk (*). The die photomicrograph with the circuit elements identified is included as Figure AlO-6.

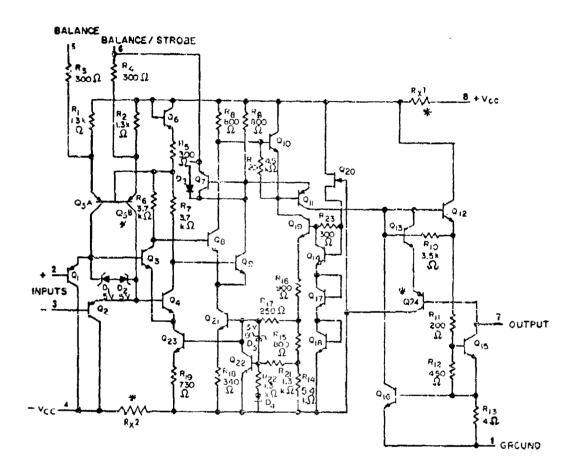
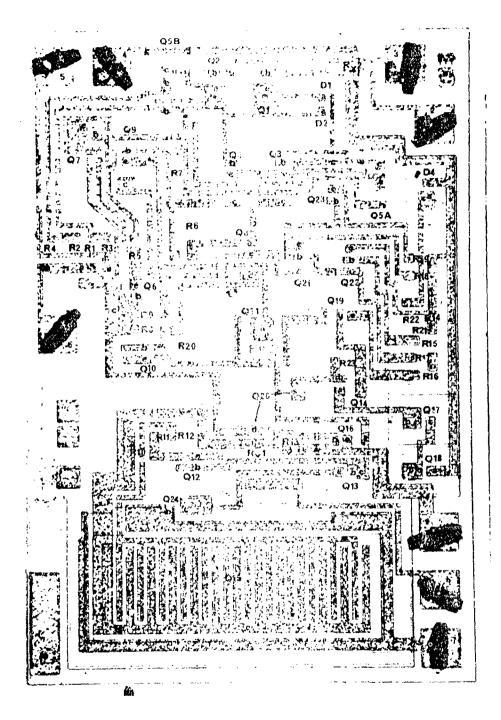


FIGURE A10-5 - SCHEMATIC DIAGRAM



130X

S/N 311

FIGURE 10-6- DIE PHOTO

E. COMPONENT DESCRIPTION

An examination of the die surface was conducted after removal of glassivation and metalization to determine the structure of each circuit element.

 TRANSISTORS (Transistors listed together share a common N type collector or base diffusion)

<u>Vertical NPN</u>	Vertical PNP	<u>Lateral PNP</u>	N Channel J-FET
Q3 Q4 Q6*,_Q10 Q7*, Q9 Q8 Q12 Q13*, Q16 Q14 Q15 Q17* Q18* Q19 Q21 Q22	Q1 Q2	Q5A Q5B Q11	Q20

*diode connected transistors

2. DIODES

<u>PN</u>	Diodeconnected NPN transistor
D1 D2 D3	D4
D5	D3 Removed

3. RESISTORS

<u>P</u>	N+
KI thru R12 R14 thru R23	R13 Rx1 Rx2

F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-STD-883, Method 2010.3.

APPENDIX B

ELECTRICAL TEST CONDITIONS

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TABLE E1. INITIAL/FINAL AND INTERIM TESTS FOR MIL-M-38510/10104 & MIL-M-38510/10107

PARAME) ER	"	AL/FINAL T #'S		INTERIM TEST #
	25°C	125°C	-55°C	25°C
v ₁₀	1, 2, 3, 4	25, 26, 27	46, 47, 48	1, 2, 3, 4
110	5, 6, 7, 8	31, 22, 33	52, 53, 54	5, 6, 7, 3
+I is	9, 10, 11, 12	37, 38, 39	58, 59, 60	9, 10, 11, 12
-1 1g	13, 14, 15, 16	40, 41, 42	61, 62, 63	13, 14, 15, 16
4PSRR	17	-	 -	17
-PSRR	18	-	-	16
CMR	19	-	-	19
V10 ADJ(+)	20	-	-	20
V10 A7J(-)	21	-	-	21
105 (+)	22	43	60	22
105 (-)	23	44	85	23
PD	24	45	56	24
Vopp	67, 68	77, 78	87, 80	67, 68
+A _{VS}	69, 71, 73, 75	79, 81, 83, 85	89, 91, 93, 95	69, 71, 73, 7
-A _{VS}	70, 72, 74, 76	80, 82, 84, 86	90, 92, 94, 96	70, 72, 74, 7

TABLE B2. CHARACTERIZATION TESTS FOR MIL-M-38510/10104 & MIL-M-38510/10107

-		CHARACTERIZATION TEST #'S	
PARAMETER	25°C	125°C	-55°C
TR	97, 93	108, 109	115, 116
SR	99, 100	110, 111	117, 118
t _s *	106, 107	113, 114	120, 121
ΔV ₁₀ /ΔΤ		28, 29, 30	49, 50, 51
ΔΙ ₁₀ /Δ ^γ		34, 35, 36	55, 56, 57

^{*} DEVICE 38510/10107 ONLY

TABLE 83. TEST SPECIFICATIONS FOR MIL-M-38510/10! (continued)

	1		É			-	٠,			-				-	·\$ -						Ğ	<u>.</u> :	PE .	۳ د	ζ.	.¢	2	_	-
-	\$	K PN	0.5+			-	0.			-	2,0			•	250			•	100	100	:	:		-12	55	580	+7.0		
10-	Limits	ניון	0.4-			•	-40			•	0			•	0	-		-	-100	-100	98	7.5	7.5	-40	21	ō.	-7.0		•
		ž	40.5			•	÷0.2			•	5.0			-	5.0			-	9:	16		:		-2.0	20	24	1 .0		•
10.	Limits	E	6.0			-	-0.2			-	-0.1			•••	- 0		_	-	9 -	21-	95			-15	2.0	2	0.1-		•
	≯ 1		VCH * -15 V 1/	-	l"		3	↓ 	A O = 83	-	ن ح	-	h C = 20h	 	 		i	H	+>_f = 10 V.	+VCC = 20 V,	VCK = +15 V			1 ±V _{CC} = ±15 V, 5 sec. mirimum	 		VrW = -15 y 1/	VCH = +15 V	-
	~	ē	-	2	m		~	10	<u></u>	37	6	<u>۱</u>	E	Ë	٦	27	2	9	1:	8	2	20	₹	22	22	24	52	56	27
-134	570-883	ne thed	1004			-o-	1603	_		-	4001	_		-	1691		 	_	4003	4/303	40v3			3011	1105	4905	4001		-
	Set S		7.0				51,	<u>-</u>		··· Par	1,14	:			-I-			~*	4P52R	¥:5e-	C4.3	Vr0 403(+)	VIO ADJE-	100(+)5/	105(-)5/	4	4	<u>.</u>	-
	Subgroup		-	TA - 25°C																		-					2	TA = 125°C	

TABLE 53. TEST SPECIFICATIONS FOR MIL.M.38510/101 (continued)

Subgroup	Symbol	MIL STO-283	_	اج	-04		-07 Li-1ts	,	Unit
		method	٠٥٢ -	OTHERMISE SPECIFIED.	, Kin	K9X	E.	, C.	
2	3V10 6/	4001	28	ay ₁₀ /a [†] -	-5.0	0.2	-15	+15	20/44
1 • 125°C	-			[V _{IO} (test 25) - V _{IO} (test 1)] × 10					
			29						
				[V _{IO} (test 26) - V _{IO} (test 2)] x 10					
			음 유	- 12/0, VA					
	-	-		[VIO (test 27) - VIO (test 111 - 15	-Øss	•	⇒	•	*
	130	1007	15		-0.3	+0.3 +	25-	0,4	·ž.
-	_		35	V _{CM} = 415 V					
	•		33	\ 0	~	-(h-	-40-	•	-
	79 01 0		35	21 ₁₀ /27 *	-2.4	+2.4	-200	.282	ر ابر ا
-	; ; ;			(I ₁₀ (test 31) - I ₁₀ (test 5)] x 10					
	_		33	6110/01					
				[I]O (test 32) - Igo (test 6)3 x 10					
			98	z110/c1 =					
		-		[1 ₁₀ (test 33) - 1 ₁₀ (test 7)] v 10		-6-	*	•	-g r.
	÷ 118	1001			-3.0	+3.0	0.1.	250	40
_				V V + 15 V					-
	-	-	33	۸ 0 = ^{۸۵} ۸		-			
	-118	1004	04	ν _{CM} 15 γ					
			4!	V 4 31 + 1 + 1 V					
_,	•	-	42	V _{CH} = 0 V	-	\$.	-	~	-
	/3(+)sc ₁	3011	43	±VCC - ±15 V, 5 sec. minimum 8/	51-	-2.0	C7-	- 12	<u>٠</u> ٤
	1 <u>0</u> 5(-)50	3011	44	±VCc = +15 V, 5 sec. minirum 8/	٦.٢	15	0.	&	Αï
	O _d	4005	45		64	35	10	240	P.E.

TABLE B3. TEST SPECIFICATIONS FOR MIL-M-38510/101 (continued)

Suboroug	3 years	FIL. \$10-893	Test	+V. * +20 Vdc, ETC R1 HAI FSS	0-		(0.		
	<u> </u>	method		OTHERWISE SPECIFIED.	ת א	49x	Z	, y y	,
E 1	9	100	46	YCH - 15 V 1/	0.1-	+9	0.7	+7.0	ω,
, FG . Y.			47	√CH = +15 ¥					
			48	V 0 - H ₂ V	-	-	•-	•	-
	7,106/	4001	49		.5.0	+5.0	-15	+15	3./Aª
	-			[V ₁₀ (test 1) - V ₁₀ (test 46)] x 12.5	_	_		_	_
	,		20						
				[V ₁₀ (test 2) - V ₁₀ (test 47)] x 12.5					
			15						
		-		[V ₁₀ (test 3) - V ₁₀ (test 48)] x 12.5	•	•	-	-	-
	115	4601	32		9 .0-	40.4	-89	იკ•	·į -
			53	V _{CM} = +15 V J					
-		-	33	Λ O = W ³ Λ	-	*	•-	\$ =	-
	7901,7	4001	55	2110/21 a	-2.5	+2.5	905-	Çn;+	p4/'C
				[1 ₁₀ (test 5) - I ₁₀ (test 52)] x 12.5					
	i —		95	21 11/21 =					
				$[I_{10}$ (test 6) - I_{10} (test 53)] x 12.5					
			15	al ₁₀ /al =					
	-	-		[1 ₁₀ (test 7) - [₁₀ (test 54)] x ⁻ 12.5	-	-C-	-	-	-
	+1 ₁₈	4001	88	Λ _{CH} = -15 V]/	-0-	4.0	0 - -	4 63	ح ح - خ
	—		59	ΛCH + +15.V					
		-	09	V _{CM} = 0	•	1,	4	-	-
_	-1.2	4001	19	/i ^ s:- = x3/	-0.1	4.0	9.1+	00	Z -
	: -		29	V _{CM} = +15 V 1/				_	
	- -	-	63		-	~	-	-	-
	/s(+)sc,	30,1	64	±V _{CC} = ±15 V, 5 sec. minimum 3/	51-	-4.0	-55	5l- 	ę.
	/₹(-)s0 ₁	1000	99	+VCc - +15 V, 5 sec. minimum 8/	4.0	0	-15	2	7
	ع	4,905	99		2	32	<u> </u>	320	ï
	-								

TABLE B3. TEST SPECIFICATIONS FOR HIL-H-38510/101 (continued)

					3			10-	
Substant Suss	System	cT2-883	Test		Limits		Limits	its	Unit
	mi, w min	ne thos	ė	OTHERWISE SPECIFIED.	r:X	Yex	Ain	Max	
*	100	130	63	R - 15 kg	æ	0 0 0	33	:	e-gy
	3.		89	R 3 2 kg		í	32	::	ر. د ک
	ا بۇ		6	راً - غ بن ريائل م باع ٨	-		30		1704
-	1		7.0	R. = 2 ka, Vour = +15 V			90		F - 14
	3		11		હ	:	53		/^
	1		77	10 k2, Vour -15 9	æ	1	93	:	
و بفروت	١		7.3	To Vác. Volit			0.5		
	1		1	LES VOCS VOUT	,		6	i	A -: / A
			75	* 5 Vdc Vour	07		G.		/A
	, x,		9	* +5 Vdc. Vour	20		40		1/-1
3,	l	1009	2	R ₁ = 10 ka	32		34	;	و. د.
TA = 125°C			78	P = 2 KG			32		پ ^ر ت ب
	ب		79	R = 3 k2. Vour = +15 V	T		0.7	:	, ./,
	1,4,1		60	R = 2 kg, Vous = 215 V	1		3		٠/٠.
	1.		18	R = 10 kp, Voter = 415 V	3	:	40		٨//٨
	2 .		35	R 0 kn. Vour	C\$		40	:	٧/٣٠
	, Y.		83	R = 2 kg, ±4cc = ±5 Vdc, Vour " ±2 V			20		4724
	, Y.		84	9 = 2 k0 + 4 CC = +5 Vdc, 19UT = +2 V			20	:	• / •
	Y X		SB	P. = 10 KO. +VCC = +5 Vdc. VOUT = +2 V	50		છ		1/61
	\ \frac{1}{2}	-	93	R = 10 kn. +VCc = +5 Vdc. Volg = +2 V	20		8	:;	٧/٠٠
•	<u> </u>	\$0ú3	8	л. = 10 ka	32	:	*	:	Vp.p
1 - 55°C	١.,		88	8 = 2 ka			32		Vp-p
	4		r,	R, = 2 ka. Vaur = +15 4	r-		30		A'a/A
-0. to-	¥.		90	R = 2 kg, Veyr = +15 V			ટ		4/54
~	14		16	R = 70 kg. Vout = +15 V	0.5		8		۸/۳۸
	-\ \ \ \ -\	-e>	35	R = 10 kg, Vout = +15 V	67	•	20	:	V/mV

TABLE B3. TEST SPECIFICATIONS FOR WIL-M-38510/101 (Continued)

Subgroup	Symbol	Hil-	1-	*** Conditions	1 40415				1
		nethod	5.	ÖTHERMISE SPECIFIED.	Ni.o	K2X	E.	X ₂ X	,
	***	4004	66	R = 2 ka, ±4cc = ±5 Vdc, Your = ±2 V			٧	:	V/m\
	-Avs		16	R. = 2 kB. ±VC = ±5 Vdc. VOUT = ±2 V			4	;	A/n/
	5A44		36	R1 = 10 kg, +VCC = 35 Vdc. Vol.7 = +2 V	20	:	•	:	,/e/
	Y-1.5	-	95	R = 10 xa, +VC = 5 Vdc, VolT = +2 V	, 02		7	÷	1/67
	1R(t_)		97	FIG. B2.		1000	1	40	เเร
3.52	18/05)	·	98	FIG. B2.	:	9		30	, v
	(+) %\$	4002	90F	99FIG. B2. Ay - 1, VIN - 5 V to +5 V	0.1	***	32		٧/ ٤٥
	(-) 85	4002	100F	1	0.1		50		87/1
	10,3		136	FIG. B2. VIN = -5 V to +5 V				820	sc s
_	(C, Y	T -	107	V 2- = NIV .	· ·		:	800	Si Si
	TK(C)		103	1	[:	1000	:	0.5	ž.
	1P.(35)		109	TA = 125°C, FIG. 82.	;	40		30	-
	SA(+)	4002	011	7 125°C,	0.1	:	7.5	;	57/A
	SR(-)	4002	=	!	0.1		50		51/1
				VIN = +5 V to -5 V FIG. B2.					
			211						
	(t) 3		113	14 - 125°C, FIG. 82.				1200	su
	(-) \$		Pil	14 * 125°C, FIG. B2.				1200	nS
	TR(E,		511			1000		40	uS
	TR(0S)		116	İ . !		10		30	٠, ٧
	SR(+)	£004	117	;	. හි.	1	75		Y/1.5
				VIN = -5 V to +5 V FIG. B2.					

TABLE R3. TEST SPECIFICATIONS FOR MIL-M-38510/101 (continued)

Subgroup	Symbol	HIL- STD-883	Test.	Subgroup Symbol Symbol Symbol Test +VCc - +20 Vdc, FIG, Bl. UNLESS	-04. Limits	\$	-07 Limits	ts	Shift
				OTHERWISE SPECIFIED.	Kin	X S	u.W	Fax	
60 -	SA(-)	4003	318	118 IT a -55°C, ffgure 9, Ay = 1,	8		50	1	٧/د۶
				VIN * +\$ V to -5 V FIG. B2.					
			6						
	Ξ.,		120	120 1 _A * -55°C		•	:	1.00	202
- C >	(-)5	-	121	1,55°C		•	:	1203	S.

1 Vem is achieved by algebraically subtracting the common mode voltage from each supply and algebraically adding the common mode voltage to v (i.e., for Vc = -15 V, +Vcc = +35 V, -Ycc = -5 V, V = -15 V). Solution the significant power dissipation and ussociated device heating, these tests shall always be the last tests performed in any given sequence, followed by operational verification (e.g., such tests as Yopp, Ays. 7R, 5R).

Effests 28, 29, 30, 34, 35, 49, 50, 51, 55, 56, and 57, which require a read and record measurement plus a calculation, may be omitted except when subgroups 2 and 3 are being accomplished for group A sampling inspection and groups B and C endocint measurements.

In the five second minimum test duration for interest that apply only for group A sampling inspections and groups B and C endpoint tests. For final electrical test, test duration for inside reduced to be consistent with automated test procedures provided that the 5 second test infits are guarant sed.

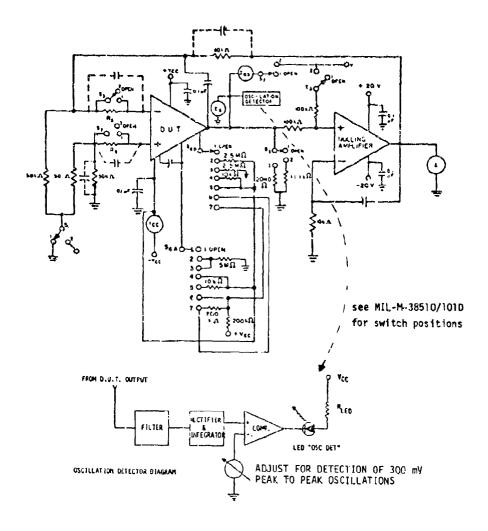
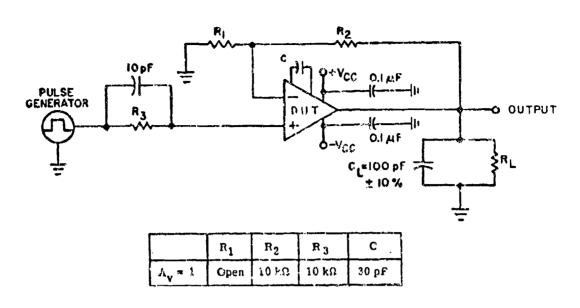


FIGURE B). TEST CIRCUIT FOR STATIC AND DYNAMIC TEST

Device type 04



Device type 07

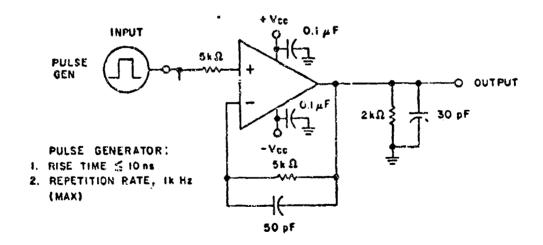


FIGURE 82. TRANSIENT RESPONSE TEST CIRCUIT

TABLE 84. INITIAL/FINAL AND INTERIM TESTS FOR MIL-M-38510/10201

125°C 11 12	-55°C 16 17	25°C 1, 2, 3 4, 5, 6
12	1 7	4 5 6
		7, 2, 0
13	18	7
-	-	8
15	20	9
	-	

TABLE B5. CHARACTERIZATION TESTS FOR MIL-M-38510/10201

PARAMETER	CHARACTERIZATION TESTS TEST #'S				
	25°C	125°C	-55°C		
T _C V _{OUT}		14	1.9		
RIPPLE REJECTION	21,22	-	-		
OUTPUT NOISE	23,24	-	147		
LINE TRANSIENT RESPONSE	25	-	-		
LOAD TRANSTENT RESPONSE	26	-	-		

TABLE B6. TEST SPECIFICATIONS FOR MIL-M-38510/10201

* ALL TESTS REFER TO FIG. B2. UNLESS OTHERWISE SPECIFIED.

Schrop	Symbol	Test	Conditions	1,510	Institution Mari	Units
1 T _A • • 25 ° C	VRLINE	1	V _{OUT} = 5 V, I _L = 1 mA V _{IN} = 12 to 15 V	,0.10	0.10	S Your
	VRIANS	2	V _{OU7} • 5 V, I _L • 1 mA V _{IN} • 9.5 to 40 V	-0.3	6.3	SVOUT
	VELINE	3	V _{OUT} = 2 V, I _L = 1 mA V _{IN} = 12 to 15 V	-0.2	0.2	€ vour
	Q.O.L.A	4	V _{OUT} = 5 V, V _{IN = 12 V} 1 _L = 1 to 50 mA	-C. 15	0.15	Vour
	VACIDAD	5	V _{OUT} = 37 V, V _{IN} = 46 V, I _L = 1 to 12 mA	0.5	0.5	Lines &
	VR LOAD	6	V _{OUT} = 7.5 V, V _{IN} = 10 V I _L = 6 to 12 mA	-0.2	, 0.2	VOUT
	VREF	7	V _{IN} * 12 V I _{HEF} * 1 mA	6.95	7.35	VDC
	los ,	8	R _{SC} = 10 Ω, R _L = 0 V _{OUT} = 5 V, V _{DI} = 12 V	45	85	mΛ
ļ	1sco	9	IL + IRFF = 0, VIN + 30 V, VOUT + VREE	0.5	3.0	mA.
7 TA + 125 °C	"RLINE	11	V _{OUT} = 5 V, I _L = 2 mA V _{IN} = 12 to 15 V	-0.2	0.2	% ∧ ^{O.\} \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\
	QV0711A	12	V _{OUT} = 5 V, V _{IN} = 12 V I _L = 2 to 50 mA	-0.4	0.4	E VO .T
	VIREF	13	I _{REF} = 1 mA, V _{IN} = 12 V	6.20	7.40	V _{DC}
	TCvour	14	V _{OUY} = 5 V, V _{IN} = 12 V I _L = 3 mA	-0.010	0.010	%/°C
	ISCD	15	1L = 1REF = 0, VIN = 30 V. VOUT = VREF	0.5	2.4	≀n A
3 T _A = -55°C	VRLINE	16	V _{OUT} = \$ V, I _L = 1 mA V _{IN} = 12 to 15 V	-G.3	0.3	", Your
	VRIDAD	17	V _{OU7} = 5 V, V _{IN} = 12 V I ₁ = 1 to 50 mA	-0.6	0.6	° VC UT
	VREF	10	$I_{RE,F} + 1 \text{ mA}, V_{ N} = 12 \text{ V}$	6.90	7.40	VDC
	1CvolT	19	V _{OUT} = 5 V, V _{IN} = 12 V I _L = 1 mA	-0.015	0.015	'∘/'c
	¹ sco	20	IL = IREF = 0, VIN = 30 V, VOUT = PREF	0.5	3.5	mΛ
4	R pple rej	21	1 = 10 kHz, CREF = 0, see figure B5.	64		dB.
TA =+25°C	Rapple rej	22	f = 10 xHz, CREF = 5 pF, see figure B5.	76	·	dB.
•	Output noise	13.7	FW = 100 Hz to 15 kHz, CHEF = C. see figure B5.	اا	· co	μV _{Iro} s
1	Output notice	24	I'W' : 160 H > to 10 kitz, CHEF = 5 h F, see figure B!	1.	7.0	hV _{1m}
	Line transient response	25	V _{IN} = 12 V, V _{OUT} = 5 V, I _L = 1 mA, R _{SC} = 0Ω, ΔV _{IN} = 3 V, see figure B4,	0	1,	m/V/V
	food tru sieut response	26	Vin * 12 1. Vont + 67, 11 * 40 mA, NSC + 06. ALL - 10 mA, configure 84.	-1.5	9	mV/mA

 $[\]underline{3}/$ To eliminate heating, test must be made in less than a 10 mS duty cycle of less than 5%. v_{OUT} is the nominal output voltage prior to application of short circuit.

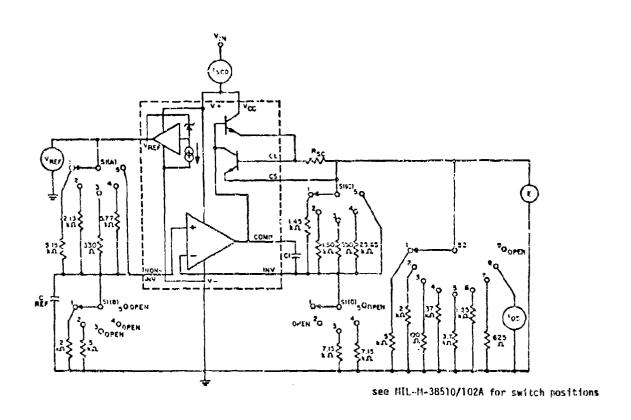


FIGURE B3. TEST CIRCUIT FOR STATIC AND DYNAMIC TESTS

The state of the same of the state of the st

RIPPLE AUSCATON (dt) = 20 log Ems NOTES:
1. For ripple rejection
Ving * 2 Vrms, 10 Mix

Paire 2 equais -750 mV, 25 pass vids, 2% daly cycle, type - 1781, - 500 ps.

3. For land transient response, \$1 in position 2 Police in 0

NOTES:

1. For line transfers response, Si is consisten 1
Fuize 1 equals 3 V high, 35 psec wide, 3% duly cycle,

1714 = 1715 = 500 as.

1. For soled Vins VINS = 0 Vins Erus 4 of 100 lis to 10 klis a soles kVins.

S. CRET is no opecified in table 32-1

%₹ ~\` 750 70 SCOPE **©** PLR HH PLESE 2 7 9 Ž Q+124 YREF ŽŽ **1**4

TRANSIENT RESPONSE TEST CIRCUIT FIGURE 84.

. B16

TABLE 87. INITIAL/FINAL AND INTERIM TESTS FOR MIL-M-38510/10304

PARAMETER		/final	INTERIM TEST #'S
	25°C	125°C	1201 % 5
v _{IO}	1, 2, 3, 4, 5, 6, 7,	30, 31, 32, 33, 34 35, 36	1, 2, 3, 4, 5, 6, 7,
¹ 10	8, 9, 10, 11	38, 39, 40, 41	8, 9, 10, 11
IIB	12, 13, 14	43, 44, 45	12, 13, 14
D _D	15	46	15
I _o	16	47	16
I_{G}	17	48	17
I _{II}	18	49	18
I _{I2}	19	50	19
+Icc	20	51	20
-Icc	21	52	21
^T cs	22	53	22
V _{IO(ADJ+)}	23	54	23
V _{IO(ADJ-)}	24	55	24
CMRR	25	56	25
v _{ol}	26, ?7, 28, 29	57, 58, 59, 60	26, 27, 28, 29
A _{VG}	92	94	92

TABLE B8. CHARACTERIZATION TESTS FOR MIL-M-38510/10304

PARAMETER	C	HARACTERIZATION TEST #'S	ON
	25°C	125°C	-55°C
t _{RLHC}	98	98	98
t _{RHLC}	99	99	99
tRLHE	100	100	100
tRHLE	101	101	101

TABLE B9. TEST SPECIFICATIONS FOR MIL-M-38510/103

Sugress	Symbol	list no.	Condition & V	Line	N1	Urit
- ,		i	Ny 501, VIC + 0, + VCC + +15V	-4	+4	nı V
TA - #5°C		1	ns + son vic + -13.5V; + VCC = +15V	-4	÷4	ωY
1 1		3	RS . 500, VIC : +12V; + VCC = +15V	-4	+4	m Y
	1		115 - 5011 VIC + 0 VCC - 12 5V	-4	+4	m Y
		- 5 - 6 7	It Report tests 1, 2, and 3 with BALISTB and BAL connected to 1 VCC	-5	+5	nı Y
	110		RS + 100 x12, VIC + U + VCC + +15V	-10	+10	nA
	Ĭİ	<u>-</u> -	ns + 100 kg; V1C + -13.5V; ± VCC = ±15V	-10	+10	r.A
	1 1	10	HS . 100 kH, VIC . +1 2V; + VCC = +15V	-10	+10	n.A
1		11	Regical test 9 with BAL/STD and BAT connected to +VCC	* *	+25.0	rΑ
	(10	12	1VCC - 115V, VIC = 0	·	+ 0.1	11/4
		13	·Vcc · ·15V. Vic · -13.5V	-150	+ 0.1	~~
	1	11	**CC * *15V. *IC * 17V	-150	+ 0.1	r۸
	P _D	15	$P_D = 15 (/+I_{CC}/+/-I_{CC}/)$	30	270	шW
	40	16	-VCC + 18V, VID + \$ INV	0	500	~
1	¹G	17	-VCC - 118V, Vm - 5 mV	10000	0	nA.
	1,1	18	'ACC . 1/8A	0	100	r.A
	112	19	1,ACC - 1/9A	0	100	nA
ļ	• lce	20	1VCC • 115V	0.5	5.0	m.A.
1	·lcc	21	+VCC = +15V	-4.0	-0.5	niA
TA - 25°C	los	22	10 ma maximum froi duration, 1900 * 1159	70	200	r:A
	VIQ(ADJ)+	23	1 VCC - 115V, VIC + 0	4.0	-	n.V
1	VIO(ADJ)-	24	, VCC - :15V. VIC . 0	4.0	-	717
 	CMIL	25	:Vcc - :15V. Vic + +12V and -13.5V	80		dВ
	VOL	26	. VCC + 4 5V, -VCC + 0, VIN = 0.5V, VD = 6 n/V	0	400	ın Y
1		21	*VCC * 4 SV. 'VCC * 0, VIN * 3.0V; VID * 6 F V	0	400	n. 7
		28	1VCC + 115V, VIN + 12V; VIO = 7 mV	0	1, 500	n, Y
		29	"VCC = 115V. VW 13V; VID = 7 mV	0	1,500	w,
TA - +125°C	V _{IO}	30	NS + 500, VIC + 0, 17CC + 1154	-3	-3	m.7
1	li	31	$n_{S} + 509. v_{1C} + -13.5V; \pm V_{CC} = \pm 15V$	-5.5	+5.5	nı V
ļ		32	Rs + 500 Vic + + 12V; + VCC = +15V	-5.5	+5.5	mΥ
}	1 1	33	75 + 500, VIC + 0, 17 CC + 12 5V	-5.5	+5.5	71.1
1	i 1	1	Repeat tests 31 .32 . 33 with DAL/STB and BAL	C 5		nıv
	+	3.5	Repeat levis 31,32, 33 with DAL/STB and BAL connected to VCC	-5.5	+5.5]
	2V10/AT	37	2V ₁₀ , V ₁₀ (test 41) - V ₁₀ (test 4) 2T 100 C	-25	+25	u v / *
	110	38	RS - 100 MR, VIC - 0, 1VCC - 115V	-10.	0+10.0	~~
		39	$n_{S} = 100 \text{ km} \text{ V}_{IC} + -13.5 \text{V}; \pm \text{VCC} = \pm 15 \text{V}$	-10.	0+10.0	nA
		10	Rs - 100 km VIC + +12V; ± VCC = ±15V	-10,	0+10.0	2.4
•	ļ 1	41	Repeat tost 39 with BAL. STB and BAL connected to + Voc	-50.	0+50.0	ا مد

^{*} Indicates changes proposed for MIL-M-38510/10304 are snown.

TABLE BIO. TEST SPECIFICATIONS FOR MIL-M-38510/103

USE FIGURE 86. UNLESS OTHERWISE NOTED

_	I	_]	Lin	1118	Unit
Subgroup	\$ymbol .	Test ND.	Conditions	Mith	Max	UNIC
TA - 125°C	Aljo/aT	42	410 to ftest 49) - f10 (test 8) AT 100°C	-700	+700	7 4/°C
	l i B	43	*VCC * +15V. ViC * 0	-100	+0.1	nl
		**	=vcc + 115V, vtc13.5V	-100	+0.1	π.Α
	•	43	1VCC + 115V. VIC + +12V	-100	10.1	n.A
j	P_{D}	45	$P_D = 15(/+ I_{CC}/+/-I_{CC}/)$	3.1	210	D(h)
	lo lo	47	±VCC + 118V, VD + 5 aiV		500_	14
	lc	48	4VCC + 118V, V D + 3 mV	-100	0	uA
	111	- 45	±VCC = 138V	0	500	n.
	112	50	1Vcc = /18V	0	500	~
	+ \cc	51	1Vcc = 115V	0.5	4.0	ns A
Ì	-tcc	52	#VCC = 115V	-3.0	-0.5	173
ļ	los	53	10 ms maximum test duration, AYCC = s15V	50	150	n A
	V10(ADJ)+	54	*VCC * +15V; V(C = 0	4.0	l	mγ
}	VIO(ADJ)-	25	*YCC = (15V; V(C = 0	4.0	1	mΥ
}	CMR	36	*VCC * +15V; VIC * +15V and -14.5V	75	ļ	40
	VOL	57	- VCC - 1.5V, -VCC - 0, VIN - 1.5V, VID + 8 MY	0	100	νıν
		58	. VCC - 4 5V: -VCC - 0, V(N - (.OV, V(D - 8 mV	0	100	m٧
1		59	*VCC = 115V, VIN = 13V, VID + 5 mV	0	2, 500	m∨
	<u> </u>	60	4VCC + +15V; VIN = -14V, VID = 5 mV	0	1,500	mv.
		61	RS - 500, VIC - 0; =VCC - 415V	-3	• 3	m''

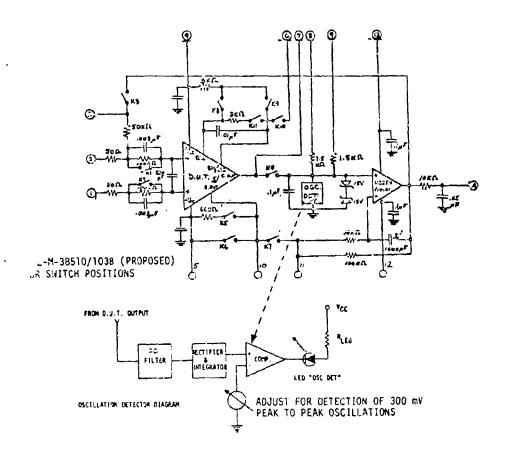
^{*} Indicates changes proposed for MIL-M-38510/10304 are shown.

TABLE BIL. TEST SPECIFICATIONS FOR MIL-M-38510/103

USE FIGURE P6. UNLESS OTHERWISE NOTED

Baterup	Sy: =1st4	Yes: He.	Conditions		eld Hila	Alax	Uest	Ì
74 - 33°C	Avc	11	35V (hrow h z) x () loud		150		V/niV	-
123°C	Avc	••	35V through a 1 kill load		35		V/ni¥	1
	\						·	
PA TUC	HERC	19	VOD + 3 MV, 3VIN + 106 MC SEE FIGURE	<u>B7.</u>	ļ	300	2.5	
7	hin.c	¥9	VOD . \$ mV; \$VIM . 190 mV. SEE FIGURE	B7.	1	300	na na	Ì
- 1 1	hane	106	VOD . S mV, &VIII - 107 K.V. SEE FIGURE	88.	:	406	ns.	ļ
_	hun.c	101	VOD - 1 e.V. AVIN - 100 MV. SEE FIGURE	B8.	L	1, 100	41	
•	4HLHC	98	VOD . \$ mV. AVIN . 100 MV SEE FIGURE	B7.		500	D.E	ľ
TA 135°C	HALL	99	VOD - 3 mV. AVIN - 163 mV. SEE FIGURE	B7.		450	R.S	1
]]	THE STATE	100	Von W. AVIN - 100 MV. SEE FIGURE	88.		2.500	PE	į
}	IMITE E	101	VOD - 3 m/V; AV(N - 100 mV. SEE FIGURE	88.		3,500	N.	1
TA59"C	INLITO	9µ	VOD . B MY: AVIN - 100 MV SEE FIGURE	B7.		106	8.5	Ī
17. 21.0	THI/LC	21	VOO - \$ mV: 4VIH - 100 mV. SEE FIGURE	B7.		300	84	
	truit.	106	VOD - \$ mV; AVIH - 100 mV. SEE FIGURE	63.		800	W.S.	
	'mu.E	101	MOD a Saiv: 4VIN . 100 mV, SEE FIGURE	88.	1	1, 100		1

^{*} Indicates changes proposed for MII-M-38510/10304 are shown.



FIGURF B6. TEST CIRCUIT FOR MIL-M-38510/10304

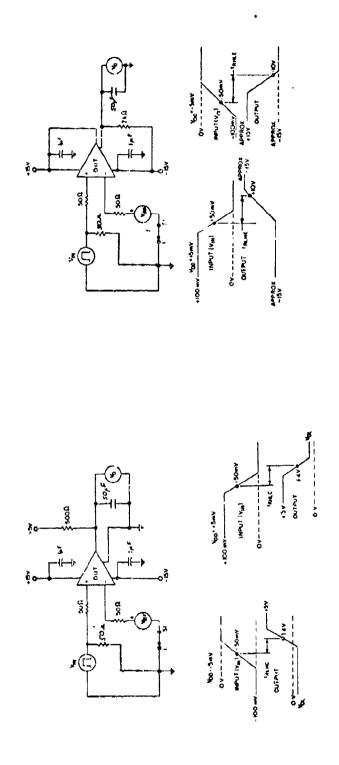


FIGURE B8. RESPONSE TIME TEST CIRCUIT AND

FIGURE B7. RESPONSE TIME TEST CIRCUIT AND MAVEFORMS

FOR COLLECTOR OUTPUT. (DEVICE TYPE 04)

MAVEFORMS FOR EMITTER OUTPUT.

(DEVICE TYPE 04)

B23

TABLE B12. INITIAL/FINAL AND INTERIM TESTS FOR MIL-M-385'0/10701

			INTERIM	
PARAMETER	25°C	125°C	-55°C	TEST #'S
VRLINE	6	21	37	6
V _{RLOAD}	7	22	38	7
Your	1, 2, 4	16, 17, 19	32, 33, 35	1, 2, 4
ISCO	9, 10, 11	25, 26, 27	41, 42, 43	9, 10, 11
ÁISCD	12, 13	28, 29	. 44, 45	12, 13
Ios	14	30	46	14
VSTART	15	31	47	15

This table refers to tests specified in this appendix. These tests are in accordance with the proposed changes in MiL-M-38510/10701.

TABLE B13. CHARACTERIZATION TESTS FOR MIL-M-38510/10701

PADAMETED		CHARACTERIZATION TEST #'S	***************************************
FARAMETER	25°C	125°C	-55°C
Δ <u>ν</u> ₀ υτ	-	24	40
TUÖV <u>A</u>	48	52	55
. No	49	-	-
AVOUT AVIN	50	53	56
Δ <u>γ</u> ΙΓ _∇ ΛΟΠ <u>λ</u>	51	54	57
ICL	58	-	-
TJ(SH)		59	-

This table refers to tests specified in this appendix. These tests are in accordance with the proposed changes in MIL-M-38510/10701.

TABLE B14. MIL-M-38510/10701 SPECIFIED TESTS/LIMITS

SUBGPOUP	SYMBOL	TEST NO		(FIGURE B9. WISE SPECIFIED) LOAD CURRENT	LIMI MIN	TS MAX	UNITS
1	v _{out}	1	V _{IN} = 7V	I _L = -5mA	4.80	5.20	٧.
T _A = 25°C		2	Y = 10V	I _L = -0.5A			
		4	V _{IN} = 35V	I _L = -50mA	+	\ ₩	1
	V _{RLINE}	6	- 7V <u><</u> V _{IN} <25V	I _L = -5mA	-20	+20	mV *
	V _{RLOAD}	7	VIN = 10V	-0.5A <u><</u> I _L <u><</u> -5mA	-50	+50	mV ≠
	ISCD	9	V _{IN} = 71	I _L = -5mA	-10.0	0	mA ·
		10	V _{IN} = 25V	I _L = -5mA			
		11	V _{IN} = 7V	I _L = -0.5A	+		+
	<u>ai</u> scd (Line)	12	7 <u>y<</u> v _{±N} <25y	I = -5mA	-0.8	+0.8	mA.
	AISCD (LOAD)	13	V _{IN} = 7V	-0.5A <u><</u> I _L <-5mA	-2.0	0	пA
	tos	14	V _{IN} = 10V.		-0.7	-0.1	A =
*	V _{START}	15	SEE FIG Bll.		-	9.0	٧
7 _A = 125°C	Vout	16	Y _{IN} = 74	I = -5mA	4.75	5.25	V •
, A]	17	V _{IN} ~ 10V	I _L = -0.5A	4.50		
	<u> </u>	19	V _{IN} 10 35V	I_ = -50mA	4.75	1	+
	· VRLINE	21	7V <u><</u> V _{IN} <25V	I_ + -5mA	-25	+25	mV •
	Y _{RLOAD}	2.2	V _{IN} = 10V	-0.5A <u><</u> I _L <-5mA	-500	+500	mV *
	τιμονδ	24	V _{IN} = 7V ·	I _L = -5mA	-1.25	+1.25	mV/*C *

^{*} INDICATES TEST (OR TEST LIMIT) CHANGES FROM EXISTING MIL-M-38510/707G1 SHEET, AND SHOWS TESTS (OR TEST LIMITS) IN ACCORDANCE TO THE NEW PROPOSED SPECIFICATIONS.

TABLE B14. MIL-M-38510/10701 SPECIFIED TESTS/LIMITS (continued)

SUBGROUP	SYMBOL	TEST NO		•	LIMI MIN	TS MAX	UNITS
2		26			~10.0	0	
7 _A = 125°C	Isco	25	V _{IK} = 7V	I_ = -5m/i	10.0	i	
		26	V _{IN} = .25V	I, # -5mA		1 1	
		27	V _{IN} - 7V	I _L = -0.5A	+	+	+
	AISCD (LINE)	28	7v <u>≤</u> v _{Ih} ≤25v	ic - bank	-0.8	0	MAX.
	AISCD (LOAD)	29	V _{IN} = 74	-0.5A <u><1, <</u> -5mA	-0.5	0	#A
	1 _{ús}	30	V _{IN} = 10V		-0.7	-0.1	A 3
	VSTART	31	SEE FIG BIL.		-	9.0	٧
3 T _A = -55°C	Yout	32	V ₁₄ = 7V	I _i = -5πA	4.75	5.25	٧.
1 '^		33	V ₁₀ = 10V	J • -0.53			
		35	V _{3N} = 359	I = -5(ImA	+		*
	V _{RL INE}	37	74 <u>44: N</u> 4234	! = -SmA	-25	+25	#/ ·
	RLOAD	58	A 14 = 104 -	-0.54<1_<-5#A	75	+75	ev *
	TUOVA	40	V _{1H} = 7V] = -5n/\	-1.25	+1.25	mV/*C*
	Isco	41	V _{1N} = 7V	I. = -5mA	-10.0	0	mA *
	1	12	V _{IN} " 25V	I,5mA	7 i		
		4.5	V _{IN} 4 74	-0.5A · I] ∤ [+	4
	AISCO	41	2A [₹] A [™] ₹52A	1 ~ -5mA	-0.8	()	eA.
	AISCO (LOAD)	45	A TM = 3A	-0.5<7 <- 5.mi	-0.5	0	üΑ
	I _{U\$}	16	V _{II} = 10V		-0.7	-0.1	A o
	VSTARY	47	SEE FIG BII.		-	0	٧

^{*} Indicates test (or test limit) change, from existing MIL-M-38510/10701 sheets, and shows tests (or test limits) in accordance with the new proposed specifications.

TABLE B14. MIL-M-38510/10701 SPECIFIED TESTS/LIMITS (continued)

6 1111 00 0112	62150	TEST	CONDITIONS		LIMI	TS	
\$UBGROUP	SYMBOL		(A ^{IM} = 10A)	NOTES	MIN	MAX	UNITS
TA = 25°3	AVIN .	48 .	I _L = -50mA	See Figure BlO. 4VIN = 1Vrms BW=10Hz to 100KHz	60	-	d8
	³⁴ 0	40	§ = -50mA	See Figure 810. BW = 10Hz to 100KHz	•	120	hA *
	TUCVA NIVA	50	I _L = -1mA	See Figure B12.	*	4.0	mV/V ±
	AIL	51	I _L = -40mA	See Figure Blo.	•	1.0	mV/mA *
TA = 185°C	7AO∩1. ∇AIN	52	I _L = -50mA	See Figure Bl2. AYIM = 1Vrms BM=10Hz to 100KHz	60	-	dB
	<u>×1¼</u> γγουι	53	I _L = -1mA	See Figure B12. AVIN = 3V	-	4.0	mV/V T
•	43L AAGUT	54	I_ = -40mA	See Figure Blo.	-	1.0	mV/mA · *
7A -55°C	TUCAN VAIR	55	Î <u>L</u> ≈ -50πA	See Figure BlO. OV _{IN} = 1Vrms BW=10Hz to 100KHz	60	-	₫₿
	AVOUT TUOVA	56	IL = -1mA	See Figure B12. AV _{IN} = 3V	•	4.0	mV/V
	11 AP	57	I = -40m/s	See Figure B12.	-	1.0	mV/mA '
7 7 = 25°C	[ICL	58		See Figure 813.	-1.0	-0.7	A
TA * 135°C)J(SH)	59	I _L = -578	See Figure B14.	165	185	°C *

^{*} Indicates test (or test limit) changes from existing MIL-M-38510/10701 sheets, and shows tests (or test limits) in accordance with the new proposed specifications.

^{**} Indicates new test.

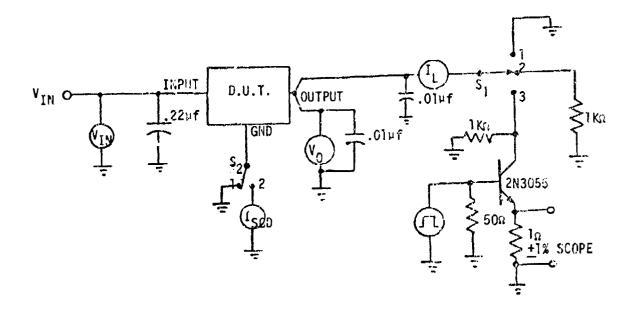


FIGURE B9. TEST CIRCUIT FOR MIL-M-38510/107

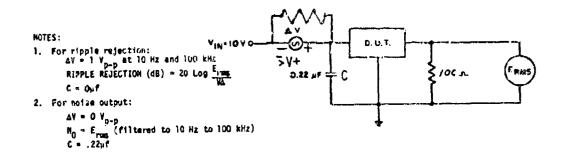
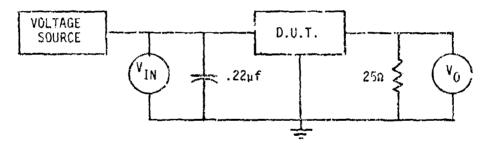


FIGURE BIO. RIPPLE REJECTION & NOISE CIRCUIT



Voltage source shall be a variable power mappiy expable of producing the following invariantees:. Device shall burn on at $V_{\rm IN} \leq 8$ V and shall remain on when the input is returned to 7 V.

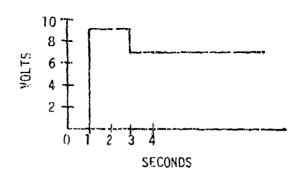
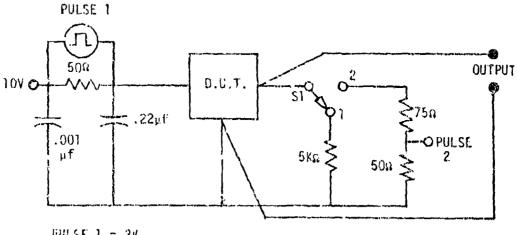


FIGURE 811. START-UP INPUT VOLTAGE TEST CIRCUIT



FULSE 1 = 3V PULSE 2 - -750mV

FIGURE 812. TRANSIENT RESPONSE TEST CIRCUIT

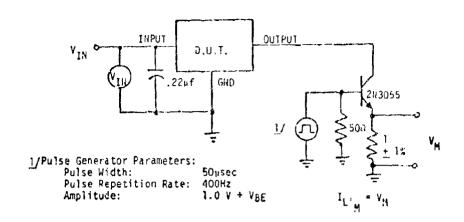
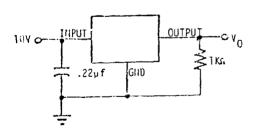


FIGURE B13. CURRENT LIMITING TEST CIRCUIT



The temperature chamter shall be stabilized at T_A = 165°C. The temperature shall be increased to T_A = 185°C over a 10 minute period and allowed to stabilize at T_A = 185°C. Accept/Reject Criteria: At T_A = 165°C; V_O must be \geq 4.6 V. At T_A = 185°C, all devices must be shut down; V_O < 1.0 V.

FIGURE B14. THERMAL SHUTDOWN TEST CIRCUIT

APPENDIX C
PARAMETER CHARACTERIZATION

APPENDIX C PARAMETER CHARACTERIZATION

Electrical parameter measurements were performed initially on all devices, and also during and after life tests.

The final electrical parameter measurements were compared to the initial results to detect any shift in parameter values. These results are shown in Tables C1 through C10.

An examination of the data was made by comparing manufacturer to manufacturer differences in initial data and comparing initial and final life test parametric data of each device type. This comparison of initial/final parametric data of each device type revealed only minor shifts in the parametric values. Where apparent differences in parameter values were noted, the control data also shifted indicating test set drift or variations due to test set recalibration. Also, comparison of the initial data to cells which have only a few survivors is not completely valid. In those cases, individual device parameter values were examined at each test time, and no major shift in values was noted. Differences in the gain parameters (±A_{VS}) were noted in the manufacturer to manufacturer comparison of MIL-M-38510/10104, MIL-M-38510/10707, and MIL-M-38510/10304 device types. A study of the transfer plots for these devices showed that the curves were nonlinear and that the two-point dc electrical measurements are not a valid indication of open loop gain. A further discussion of the open loop gain differences can be found in Appendix E.

TABLE C1. MANUFACTURER A MIL-M-38510/10104 25°C PARAMETER CHARACTERIZATION

							FINAL ACCE	LERATED L	IFE TEST C	ATA		
		Limi		Initia	0.4.	225°C 400	00 KRS. RTS = 12	200°C NO. OF P	4000 HRS. ARTS - 13		4000 HR5. ARTS - 23	
Parameter	lest Ka.	MIN		Mean	Sigma	Mean	Sigma	rlean	Sigma	Hean	Signa	Units
v ₁₀	Λ	.6.5	+0.5	-0.003	0.137	-0.132	0.095	0.603	0.125	-0.022	0.158	n-V
+A _{VS}	69	80		865.8	1568	3745,142	5984.629	2453.999	4766.953	496.480	194,150	VzinV
-A _{VS}	70	80		203.5	87.26	166.405	79.274	239.161	79.717	142.351	45.134	VyeV
+A _{VS}	71	20		252.6	255.2	269.178	220.429	3085.472	11724.695	203.711	136.622	V/ TY
-A _{VS}	72	20		191.4	47.95	134.7%1	56.992	144.252	39.944	124.384	43.304	V/a:V
110	1.	-0.2	+0.2	-0.007	0.026	0.004	0.018	-0.013	0.017	-0.009	0.029	nΑ
1 1B	\sqrt{y}	0.1	2.0	1.056	0.305	0.979	0.147	0.957	0.140	1.099	0.236	èп
-11B	A	0.1	2.0	1.063	0.302	0.980	0.151	0.970	9.140	1.105	0.246	nA
+PSRR	17	0	16	2.438	0.903	-2.525	0.944	-2.612	0.868	-2 445	1.765	u Y / Y
-PSRR	18	0	16	1.118	2.078	2.304	1.638	-0.839	2.583	2,680	2.352	V VV 4
CMRR	19	96		121.124	7.240	119.923	5.018	125.291	8.081	113.996	4.008	dЗ
+10\$	22	15	-2,0	-9,033	0.627	-9.345	0.208	-8.749	0.423	-9.228	0.473	/un
-I _{0S}	23	2	20	12.289	4.302	13.835	0.856	8.647	3.064	14.046	2.425	m۸
PD	24	2	24	13.958	2,584	14,462	1.168	12.498	2.099	14.825	0.861	m W
v _{op+}	67	16		19.167	U.078	19,459	0.016	19.439	0.035	19,441	0.091	Vρ
v _{0P-}	68		16	18.914	0.064	-18.732	0.027	-18,706	0.044	-18,710	0.035	Vp

Average values for Test Numbers 1-4.

Average values for Test Numbers 5-8.

Average values for Numbers 9-12.

Average values for Test Numbers 13-16.

TABLE C2. MANUFACTURER B MIL-M-38510/10104 25°C PARAMETER CHARACTERIZATION

							FINAL A	CCELERATE	LIFE TES	TUATA		
	lest	Limi	ts	Initial	Data	225°C 1	000 HR\$	200°C NO. OF F	1000 HRS PARTS - 5	175°C 10	000 HRS	
Perameter	No.	HIM	MAX	Hean	£1gma	Mean	Signa	Hean	Signa	Mean	Sigma	Units
¥10	\overline{W}	0.5	+0.5	-0.007	0.204	0.015	0.055	0.708	0.179	0.036	0.140	mγ
+Ays	69	80		1,614	1.892	228.892		1163.350	1834.343	16 '34 . 512	14315.242	V/mV
-Ays	70	80	· • •	1,920	3,039	174,267		2052.478	2187.422	1129,867	575.7C4	V/mV
+AVS	71	20		1,120	1,373	170.314		397.930	109.976	653.753	. 267.677	V/mV
-A _{VS}	72	50		2,984	8,659	152 987		1172.205	1398.600	2509.917	1647.569	V/mV
110	A	0.2	10.2	0.012	0.041	-0.022	U,003	-0.050	0.052	-0.008	0.012	nA
118	\triangle	0.1	2.0	1.067	0.413	0.633	0.045	0.767	0.091	0.687	0.053	nΛ
-1 IR		0.;	2.0	1.078	0.415	0.686	0 074	0.757	8.107	0.699	0.057	nA
+PSRR	17	0	16	0,470	1,635	4.551		-0.286	1.370	-0.762	1.635	₽ V / V
-PSRR	18	0	16	1.707	0.925	2.536		2.264	1.770	2.008	0.807	₽V/V
CMRR	19	96		124.7	8 916	116.137	j 1	125.644	5.694	117.269	2.757	dВ
+1 _{US}	22	15	2.0	-5.406	0.155	5.279		-5.227	0,126	-5.233	0.233	กห้
-105	23	2	20	11.41	0.269	11.314		11.167	0.155	10.810	0.118	mA.
P _U	24	2	24	11.08	6.874	10.268		10.883	0.492	10.980	0.351	m¥
VOP+	67	16		18,493	0.690	18.951		18,947	0.027	18,918	0.031	V _p
Vup-	68		16	-18.836	0.056	18.739		-18,732	0.031	-18,693	0.022	V _P

Average values for Test Numbers 1-4.

Average values for Test Numbers 5-8.

Average values for Test Numbers 9-12.

Average values for lest Numbers 13-16.

TABLE C3. MANUFACTURER B MIL-M-38510/10107 25°C PARAMETER CHARACTERIZATION

							FINAL	ACCEL "KAT	ED LIFE TE	ST DATA		
	_					175°C	1000 HRS.	150°6	1000 HAS.	125°i	1000 HRS	
-	Test	Limi	its	Initial	Date	NO. OF P	ARTS - 4	NO. OF	NO. OF PARTS - 4		PARTS - 6	
Parameter	No.	MIN	MAX	Kean	Signa	Mean	S1gma	Nean	Signa	Mean	51 gma	Units
v 10	Δ	4.0	+4.0	0,319	1.393	-1.062	1.370	-U.369	1.311	-0.244	1.638	mγ
+Avs	68	80		151.9	29.11	156 609	28.131	138.755	21.843	158.162	74.727	Y/mY
-Λ v s	70	80		112.0	16.46	111.004	22.457	103.808	19.014	112.673	20.133	V/mV
+A _{VS}	71	80		154.0	81.50	170.061	45.984	172.847	79.574	247.665	113.493	V/nV
-4 _{VS}	72	80		174.9	65.18	161.578	178.307	146.645	38.858	166.892	74.111	V/mV
+A _{VS}	7.3	40		169,5	98.31	180.070	57.433	161.810	3 7.531	480,114	688.503	V/mV
-A _{VS}	74	40		115.9	18.81	115,194	30.827	95.201	11.125	17.325	26.046	V/mV
+A _{VS}	75	40		123.2	70 73	135.569	36.273	218.996	183 822	224.247	119.670	V/mV
-^vs	76	40		1139.8	3037	231 .374	86.480	212.954	116.275	483.305	504.467	Y/mY
130	Δ	-40	خدر.	-0.317	6.401	11.331	17.257	-1.118	3.596	-6.003	8.296	nA
+IIB	Δ	+1	250	108.0	23.82	147.399	51,231	125.516	25.903	121.255	29.962	nA
-I _{1B}	Δ	֓	25ú	111.2	24.05	139.201	37,151	127.563	25.093	128.444	31.828	nA
+PSRR	17	0	100	-26.08	10.37	-22.811	11.245	-31.069	12.942	-21,349	11.902	μ Υ/ Υ
-PSER	.в	0	100	-14.95	6.447	-18.760	2,740	-16.099	16.420	-10.096	13.710	μV/γ
CHR	. و	80		105.3	8.658	110.746	18.444	108.061	11,605	107,764	10.032	₫B
V LOADJ(+)	20	7.5		12.52	0.830	12.905	U.802	12.889	0.534	13.161	0.843	m/
Y10403(-)	21	7.5		-12.68	0.844	-12.896	0.64/	~13,086	0.652	-13.368	0.810	mY
I ₀₅ (+)	22	-40	-12	-31.18	1.205	-30.663	0.718	-30.811	0.743	-30.656	1.849	mA.
105(-)	23	12	55	39.42	1,553	40.236	2.243	33.340	1.771	37.988	3.292	πΑ
Po	24	10	230	262,6	9,77	261.452	5,156	256,111	1.507	260,301	21,113	n#
¥ _{OPP}	57	34	}	37.77	0.117	37.930	0.022	37.813	0.027	37.942	0.073	V _{P-P}
VOPP	69	32		36.25	0.123	36.530	0.141	36.440	9.124	36,598	0,173	4-6 م-4
		1		{								Y-7

A Data listed represent average values for test numbers i through 4.

 $[\]triangle$ Data listed represent average values for test numbers 5 through 8.

³ Data listed represent average values for test numbers 9 through 12.

______ Data listed represent average values for test numbers 13 through 16.

TABLE C4. MANUFACTURER C 25°C MIL-M-33510/10107 PARAMETER CHARACTERIZATION

							FINAL ACC	FLERATEO I	1221 1111	NAYA		
		Lini		Initial Data		J		150°C 4000 HRS 110. OF PARTS - 30		125°C 4000 HRS NO. OF PARTS - 23		
Parameter	Yest No.	HIN	HV7	Mean	51982	Hean	Sigma	Hean	Sigma	Меан	Signa	Units
¥ ₁₀		-4.U	+4.0	0.053	1.273	0.673	1.561	0.273	1.239	0.537	1,374	t.iV
+A _{VS}	69	80		2068	3315	2723.077	6429.410	1716.619	2094.006	923.154	803.507	Y/mV
-A _{VS}	70	80		2966	8711	5272,578	18963.509	4675.023	16405.414	767.412	602.991	V/mV
+AVS	71	80		964.4	2321	549.678	497.054	743.035	1209.795	622.427	986.223	V/mV
-A\s	72	80		140.9	129.9	70.044	30.501	71.146	21.362	75.495	28.030	V/niV
+AVS	73	40		161.2	129.1	204,720	220,265	149.579	103.002	164,300	77.997	V/.rV
-A _{VS}	74	40		228.9	778.1	142.521	41.387	136.108	27.495	2584.124	11294.500	V/mV
+A _{VS}	75	40	ļ	525.8	1037	464.529	726.873	412.515	469.878	749.231	2221.062	V/mV
-A _{VS}	76	40] <u> </u>	738.6	1852	1150 085	2295.207	626.233	832.009	1499.613	4007.146	V/mV
110	Δ	-40	+40	. 9, 499	9.523	-5.130	9.865	-7.704	8.540	-9.13⊍	7.046	nΑ
+i'IB	M	+1	250	173.5	31,94	185,541	35.442	185.446	34.016	177.095	34,359	nΑ
-I ₁₈	4	+1	250	187.0	31.23	197.005	36.594	197.407	33.469	199.958	34.470	nА
+PSRR	17	0	100	-14.768	10.15	-18.511	10.169	-16.283	6.698	-17.778	12.359	V/V
-PSRR	18	0	100	-35,373	12,13	-35.303	12.130	-35.941	9,500	-35.185	14.001	¥/¥
CMPR	19	80		100.1	6.568	100.526	4,951	98.735	4.094	101.773	5.581	dB
V 10&401(*	29	7.5		16.92	1,193	16.828	1.654	17.114	1.026	17.364	1.203	rοV
VIOARDI(21	1.5		-16,83	1.397	-16.987	1.502	-17.360	1.389	-17.270	1.206	m∀
105(+)	22	40	-12	-30.19	1.358	-30.549	1.299	-30.893	1.168	-30.813	1,405	πıA
105(-)	23	12	55	24.94	2.533	25.093	3.239	24.694	1.835	24.759	2.238	mA
r _n	24	10	280	204.3	11.65	206.444	13.963	204.720	8.091	201.535	10,837	mW
A ^{Ook}	57	34		37.81	0.147	37,756	0.243	37.789	0.112	37.838	0.083	V _{p-p}
YOPP	68	32		36,60	0.188	35,464	0.300	36.476	0.202	36.564	0.132	, p.p

 $[\]triangle$ Average values for Test Numbers 1-4.

Average values for lest Numbers 5-8.

Average values for Test Numbers 9-12.

Average values for Test Numbers 13-16.

TABLE C5. MANUFACTURER D 25°C MIL-M-38510/10201 PARAMETER CHARACTERIZATION

	MAX 0.10 0.3	Initia? Hean -0.017 -0.117	Data 51988 0.004 0.029	200°C 4 NO. OF PA Mean -0.020	000 HRS RTS - 35 S1gms 0.007	175°C NO. OF Pi Mean -0.019	4000 HR5 ARTS - 32 51gma 0.005	Mo. OF P.	4000 HRS ARTS - 35 Stgme	Units
MIH -0.1	MAX 00.10 0.3	Mean -0.017	51gms 0.004						Signa	Units
-0.3	0.3		(-0.020	0.007	-0.019	0.006	1	1 1	
Ì	1	-0.117	0.029				0.005	-0.018	0.003	r v _{our}
Δ.2	100		0.023	-0.144	0.040	~6.141	0.025	-0.176	0.018	* Y ₀₀₁
٠,٠	10.7	-0.011	6.005	-0.015	0.009	-0.013	0.005	-0.012	0.004	* V _{0U1}
0.1	50.15	-0.011	0.009	-0.015	0.012	-0.912	0.001	-0.014	0.006	\$ V _{OUT}
0.5	0.5	0.000	0.014	-0.001	0.004	-0.002	1.001	0.002	0.002	£ V _{OUT}
0.2	0.2	0.003	0.003	0.005	0.005	0.006	יטס.ס	0.006	0.001	X YOUT
6.9	7.35	7.243	0,056	7.230	0.058	7.248	0.034	7.228	0.052	¥
0.	3.0	2.472	0.143	2.552	0.117	2.591	0.108	2.645	0.143	mA
45	85	59.19	5.217	61.760	3.001	62.628	2.426	62.737	1 922	mA
	0.5	0.5 3.0	0.5 3.0 2.472	0.5 3.0 2.472 0.143	0.5 3.0 2.472 0.143 2.552	0.5 3.0 2.472 0.143 2.552 0.117	0.5 3.0 2.472 0.143 2.552 0.117 2.591	0.5 3.0 2.472 0.143 2.552 0.117 2.591 0.108	0.5 3.0 2.472 0.143 2.552 0.117 2.591 0.108 2.646	0.5 3.0 2.472 0.143 2.552 0.117 2.591 0.108 2.646 0.143

TABLE CO. MANUFACT RER C 25°C MIL-M-38510/10201 PARAMETER CHARACTERIZATION

Data Signa	200°C 4	1000 HRS		1000 HRS	150°C (300 UZS	
	NO. OF PA	RTS - 27		,		DOC HRS	
\$1gava			NO. OF PARTS - 35		NO. OF PARTS - 35		
	Xean	Signu	Mean	51 gan:	Mean	Stgma	Units
0.011	-0.017	0.011	-0.023	0.013	-0.019	0.011	⁴ V _{COT}
0.049	-0.107	0.027	-0.127	0.038	-J.118	0.024	* v _{CU} 1
0.010	-0.012	0.011	-0.017	0.012	-0.012	טיס.ט	* AUT
0.010	-0.017	6.005	-0.012	0.006	-0,621	0.006	z vov
0.005	-0.001	0.002	-0.000	0.004	0.000	6.003	* Y ₀ 01
C.003	0.003	0.001	0.007	0.018	0.004	0.001	3 Y _{0U} 1
0.097	.7.146	C.097	7.254	0.50	/.253	c.039	٧
0.412	2.556	0.287	2.211	0.316	2.201	0.368	m \$.
2.801	60,441	2.543	60.626	1,151	61.600	1.121	mΑ
	1						

TABLE C7. MAMUFACTURER D 25°C MIL-M-38510/10701 PARAMETER CHARACTERIZATION

						FINAL ACCELERATED LIFE TEST DATA						
						250°C	4000 HRS	225°C	4000 HRS	200°C	4000 HR5	
	Tust.	Lini	ts	Initial Data		HO. OF PARTS - 32		NO. 07 P	ARTS - 32	MC. OF PAR15 - 32		
Parameter	140.	MIN	MAX	Meani	51 gas	Mean	Signa	Mean	Signa	Mean	Signa	Units
VOUT	1	4.80	5.20	5.044	0.042	5.032	0.035	5.047	0.035	5.037	3.025	Vác
YOUT	2	4.80	5.20	5,044	0.041	5.024	0.036	5.040	0.035	5.029	0.023	Vdc
Your	4	4.80	5.2J	5,029	0.044	5.035	0 035	5.051	0.035	5.038	0.024	Vdc
YRLM	6	-20	+20	17.388	1.900	-14.437	1.540	14.750	1.479	15,093	1.284	mYdr.
Y _{fo_O}	7	-50	+50	-2.790	2 626	6.219	2.103	4.563	1.967	5.438	2.703	M¥4c
(sco	9	10.0	0	7,168	0.342	-6.777	0.346	-6.890	0.214	-€.876	0.241	mA42
1 _{sco}	10	-10.0	c	-7.224	0.367	-6.684	0.357	-6.781	(.233	-6.772	0.269	wydc
i _{SCD}	ព្រ	10.0	0	-7.130	0.368	-6.627	0.346	-6.733	0.216	-6.735	9.277	пАфс
a 1 _{SCD}	12	-0.B	-c.8	-0.056	0.046	0.093	0.064	0.109	0.042	0.104	0 048	r Aác
a 1 _{SCO}	13	-0.5	0	-0.038	0.067	-0.155	0.130	-0.157	0.115	0.143	9.110	m Acc
los	14	-2.0	-0.1	-1.221	0.003	-1.226	0.000	-1.220	0.001	1.230	0.002	Ads
TRATZ	15		9.0	5.037	(1.046	5.042	0.035	5.057	0.036	5.047	0.025	Vdc:

TABLE C8. MANUFACTURER B 25°C MIL-M-38510/1070! PARAMETER CHARACTERIZATION

				•		FINAL ACCELERATED LIFE TEST DATA							
						250°C	4500 H/S	225°C 4000 HPS		200°C 4000 HRS			
	lest	Livits Initial Dita			50. OF PARTS - 32		80. OF 111K4 32		NO. 05 MARTS - 32				
Parameter	HO.	M/F	NAT.	Kear.	Sigma	Mean	Signa	Mcar.	Signa	Hour	5:900	U414x	
V _{OU} ;	1	1.80	5,20	5.039	0.061	5.015	0.031	5.019	0,055	4.999	0.045	Υċc	
VOUT	2	4.60	5.20	5.003	0.080	4,931	0.050	4,905	0,055	4.967	0.041	Ydc	
YCAST	4	4.8C	5.20	5.061	0.063	5.093	0.054	5,098	0,057	5.036	0.046	Yde	
V _{RLN}	1,	r20	۰20	5.710	2.626	7.344	2 217	2.061	1,455	(,437	1.602	m∀d¢	
¥ALO	7	-50	+50	35.639	3.510	35,031	2.779	33,454	2,466	33.500	3.270	wydc	
1sco	9	10.0	0	-4.684	0.350	-4.04;	0.376	•4.061	0,307	. 3.9%.	0 326	m\1c	
ISCD	10	10.0	0	-4.070	0.367	-5.925	0.283	-3.942	0.307	3.869	0.346	alde	
i _{scu}	: 3	19.0	0	-4.056	0.349	-3.742	0.261	-3.789	0,323	-3,757	0.344	MAGE	
41250	12	0.8	-0.8	0.014	0.047	0.115	0.044	0,118	0.033	9,136	0.936	HA.	
1 SCD	13	0.5	0	-0.028	0.028	-0.301	0.129	-0.281	0.107	-0,241	0.091	ov A cc.	
201	14	-2.0	-0.1	-0. 905	0.149	.0,910	0.138	-0.941	0.139	ase,n.	u 15#	Act	
Y _{START}	15		9.0	5.01/	0.061	5.013	0.052	5.015	0.056	4.955	0 045	Yde	
		[}	l		l			

TABLE C9. MANUFACTURER B MIL-M-38510/10304 25°C PARAMETER CHARACTERIZATION

		DATA	LIFE TEST	CELERATED	FINAL A							
	00 HRS	200°C 5	00 HRS	225°C !	00 HR\$	250°C 5						
	ART5=17	No. of P	PARTS-14	No. of I	ART5-20	No. of P	Data	initial	sits	L 11	Test	
Unit	Signa	Mean	Sigma	Mean	\$1gm a	Nean	Sigma	Mean	Max	Hin	Mo.	Parameter
8.37	0.751	3.452	0.724	2,747	1.131	2.142	0.452	-0.243	+5	-5	1-4	۷,0
en.	G.324	1.293	0.432	0.887	U.727	0.618	0.467	-0.299	+5	-5	5-7	VICR
¥/#¥	405.188	899.990	323.444	523.588	522,605	650.505	1354.266	925.260	-	150	92	*A _{VC}
¥/##	67.578	249.000	132.577	331.471	149.427	331.453	2028.147	1371.064	! -	150	93	- ¹ vc
nA	2.831	-3.921	4.474	-4.040	5,141	-3.938	1.181	1.740	+20	-20	8-10	110
nª	6.890	13.834	10.053	-8,965	13.589	-2.972	3.150	1.387	+25	-25	11	110R
n/t	13.115	-53.018	18.275	-65.936	18.245	-58.260	14.778	-53.829	0.1	-150	12-14	*1 ₁₈
n/A	11.826	-50.733	17.057	-62.689	17.726	-55.018	15.055	-55.014	0.1	-150	12-14	-118
e#	0.403	6.973	0.405	5,699	C.225	5.784	0.251	5.219	- i	4.0	23	+Y10(ADJ)
∫ -∨	0.301	-5.345	0.326	-5.13?	C.305	-5.3:8	0.266	-5.369	-	4.0	24	-V 10(ADJ)
on€	1.581	86.251	1.275	87.517	1.914	88.884	5 .946	110.727	- !	80	25	CHRR
v	0.018	0.325	0.624	0.328	0.021	0.312	0.015	0.276	.400	0	26-27	V _{OL 1}
	0.048	0.922	0.055	0.939	0.048	0.935	0.037	0.915	1.500	0	28-29	S 16A
4 ر	0.004	0.076	Ų.005	0.083	0.020	0.095	0.007	0.123	.500	e	16	10
u A	0.108	-0.029	0.815	-0.895	0.519	-0.412	1.342	-1.295	0	-10.0	17	i ₆
u A	0.001	0.069	0.003	0.071	0.004	0.072	0.003	0.048	.100	1 0	18	111
, A	0.004	0,967	0,000	0.070	0.900	0.070	0.004	U.646	.100	0	19	112
942	0.198	3.020	0.285	3.382	0.275	3.177	0,267	3.250	-5.0	0.5	20	+11c
profe	0.088	-2.063	0.178	-2.334	0.211	-2.147	0.209	-2.306	-0.5	-4.0	21	-110
mA	:2.695	139,490	15.415	140.191	13.204	129.469	12.962	140.112	200	70	22	los
erte	\$.689	152.487	13.663	171.461	14 .470	160.518	14.072	166.653	270	30	15	°D

TABLE C10. MANUFACTURER D MIL-M-38510/10304 25°C PARAMETER CHARACTERIZATION

)		ATAG T	LIFE TES	ACCELERATE	FINAL							
İ	500 HRS	200°C	500 HR	2?5°C	500 HRS	250°C						
i	PARTS-17	No. of	No. of PARTS-14		No. of PARTS-20		imits Initial Data		Test Lia			
Unit	Sigma	Hean	Sigma	Mean	Signa	Mean	Sigma	Mean	Max	Min	Mo.	Parameter
-	0.789	3.402	0.702	3.259	0.640	3.570	0.414	-0.335	+5	-5	1-4	v 10
, av	0.338	0.501	0.528	0.383	0.522	0.597	0.389	-0.743	+5	-5	5-7	V104
V/#W	577.447	17/.441	628.532	586.830	429.181	823.617	73.339	459.867	-	150	92	*Avc
V/W	534.965	362.708	757.561	1075.414	731.412	269.437	38.799	302.513	-	150	93	-Avc
nA	2,241	-1.611	2.778	-5.490	4.065	-6.592	1,661	0.678	+20	-20	R-10	110
nA.	6.855	10.027	5.382	-5.465	5.564	-9.345	4.446	3.992	÷25	-25	11	1:0R
nA.	26,778	-59.702	24.628	-54.975	27.035	-64.108	27.401	-56.3?0	0.1	-150	12-14	
nA.	29.651	-59.726	22.341	-49.865	27.491	-59.413	27.791	-57.132	0.1	-150	12-14	
es/	0.345	9.727	0.278	9.359	0.264	9.404	9.289	8.929	-	₹.0	23	+V10(VO))
ndi	0.298	-8.465	0.203	-8.190	0.256	-8.202	0.290	-8.612	-	4.0	24	-V ₁₀ (NW)
de	2.746	88.091	7.984	91.997	3.977	91.286	5.760	105.366	-	ຄວ	25	CMRR
٧	0.026	0.285	0.019	0.271	0.02ს	0.271	0.018	0.230	.400	0	26-27	VCL 1
٧	0.080	0.856	0.021	0.829	0.022	0.845	0.021	0.833	1.500	0	28-29	VOL 2
A	0.008	0.991	0.306	0.094	0.003	0.089	0.007	0.123	.500	~ 0	16	10
A	0.043	-0.011	0.046	-0.001	0.021	0.017	0.966	-0.855	c	-10.0	17	I_{G}
A	0.002	0.970	0.005	0.074	0.064	0.074	0.003	0.048	.100	0	18	1:1
A	0.002	0.076	0.040	0.079	0.002	0.070	0.003	0.049	.100	0	19	112
mA	U.239	4.106	0.191	4.079	0.221	4.225	0.244	4.113	-5.0	0.5	20	*11C
ms	0.199	-2.776	0.116	-2.707	0.191	-2.850	0.726	-2.951	.0.5	-4.0	21	-1 _{IÇ}
PA	4.245	163,947	3.848	168.893	4.335	171.275	5.014	163.697	200	70	55	105
861	12,987	205.471	6.305	203.571	12,227	212.250	13.962	211.924	270	30	15	PD

APPENDIX D

BIAS CIRCUIT EVALUATION

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1.0 INTRODUCTION

Valid accelerated life test results at ambient temperatures up to 250°C depend upon the selection of the proper bias circuit. The existing MIL-M-38510 bias circuits were evaluated up to ambient temperatures of 275°C. In those instances where the existing circuit was unacceptable, or a MIL-M-38510 circuit did not exist, several candidate circuits were evaluated to find a bias circuit that

- (a) Maintained maximum rated voltage at the device terminals over the temperature range to provide maximum acceleration of surface effect failure mechanisms.
- (b) Maintained the device current at a controlled low level to minimize failures due to thermal runaway and electromigration.
- (c) Maintained a consistent set of internal microcircuit stress (primarily voltage) conditions over the temperature range. A drastic difference between circuit node voltages at different accelerated test temperatures may invalidate subsequent calculations of acceleration factors.

2.0 MIL-M-38510/10104 (LM108A) EVALUATION

Prior to selecting a suitable bias circuit for the LM108A devices the accelerated life test bias circuit contained in MIL-M-38510/101D (15 September 1975) was updated by the circuit contained in Amendment 3 (22 February 1977) and subsequently included in MIL-M-38510/101E. The original bias circuit (as shown in MIL-M-38510/101D) did not apply maximum stress across the device, therefore the circuit configuration was updated. Operation of LM108A devices in the accelerated life test circuit shown in Amendment 3 indicated the circuit was not suitable for the LM108A operational amplifier. The circuit places 40 Vdc across the device through a 100 ohm resistor, 5 Vdc to the non-inverting input through a 1K ohm resistor, and grounds the inverting input. Two problems were experienced with this configuration: a) the 5 Vdc input voltage results in excessive input current due to transient protection diodes between the inverting and non-inverting inputs of the amplifier, and b) device output voltage would switch state (due to thermal biasing) above 150°C. Lowering the 5 Vdc input voltage to 2 Vdc reduced the input current to acceptable levels, but the device output voltage would still switch state above 150°C. Applying a 2 Vdc voltage to the inverting input of the amplifier and grounding the non-inverting input provided a fairly consistent output voltage between temperatures of 200°C and 250°C. Although the cutput is thermally biased high, previous experience had indicated that most operational amplifier failures were input related, and operating the device in this configuration was not considered a problem. The average performance of five devices in this circuit configuration is shown in Figures D1 and D2. As indicated in these figures, the output voltage is high and consistent (between 35 Vdc and 39 Vdc) at ampient temperatures above 200°C. Also, the input bias current is below 2 mA at ambient temperatures up to 250°C. Above 250°C the total device current became excessive due to thermal runaway. During step-stress testing, thermal runaway occurred at the 275°C step. These results indicated that life tests could be performed at temperatures up to a maximum of 250°C. However, when the 250°C life tests were initiated, 43% of the Manufacturer A devices drew excessive current after one half hour at 250°C. All of these devices had a 7642 date code whereas the circuit evaluation and step-stress test devices had a 7643 date code. Apparently the 7642 date coded devices were susceptible to

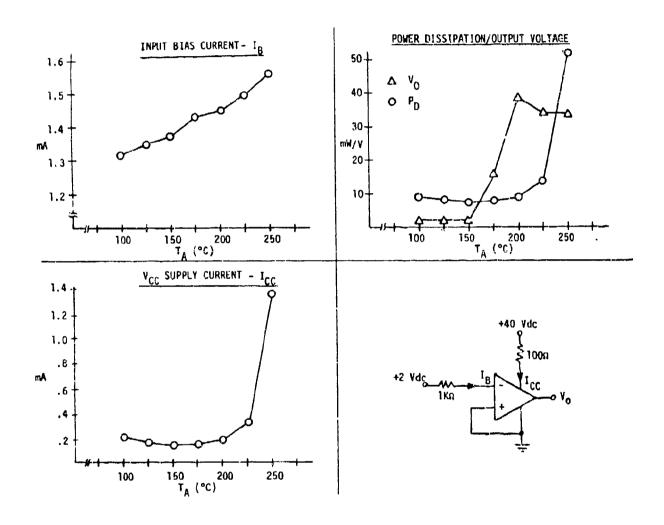


FIGURE D1. MANUFACTURER B MIL-M-38510/10104 (LM108A) CIRCUIT EVALUATION

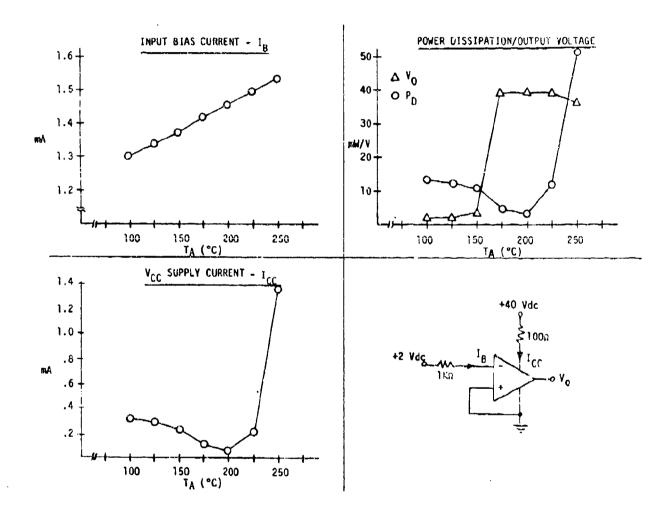


FIGURE D2. MANUFACTURER A MIL-M-38510/10104 (LM108A) CIRCUIT EVALUATION

thermal runaway at a lower temperature (250°C) than were the 7643 date coded devices, but examinations of these devices disclosed no physical difference between the devices of each date code. Consequently, the 250°C life test was immediately terminated and, after electrical testing, the devices were returned to life test and the temperature was reduced to 175°C. Thus, the LM108A life test temperatures were 175°C, 200°C and 225°C.

3.0 MIL-M-38510/10107 (LM118) EVALUATION

Operation of LM118 devices in the accelerated life test circuit shown in Amendment 3 (22 February 1977) of MIL-M-38510/101D indicated the circuit was not suitable for the LM118 operational amplifiers. This circuit is identical to the previously described MIL-M-38510/101D circuit for the LM108A, and identical problems were experienced with the LM118 (the input bias currents were excessive and the output voltage changed state). Operation of LM118 devices in the bias circuit selected for the LM108A resulted in the performance characteristics (average of 5 devices) shown in Figures D3 and D4. As indicated in the figures, the output voltage is constant up to 200°C and input bias currents are less than 1.3 mA. However, the output voltage changes state due to thermal biasing at temperatures slightly above 200°C and one Manufacturer B LM118 drew excessive current at 225°C. The Manufacturer C LM118 device did not draw excessive current unit1 250°C. Attempts to find a biasing configuration that would avoid the thermal biasing problem were unsuccessful. Two candidate circuits evaluated in attempts to avoid thermal biasing are shown in Figure D5 as Circuits B and C_{\bullet} . Also shown in the figure for comparison is the selected LM108A/LM118 bias circuit (Circuit A). Circuit B reduces the voltage across the device from 40 Vdc to 30 Vdc, but devices still experience thermal biasing slightly above 200°C. Circuit C maintains 40 Vdc across the devices by applying plus and minus 20 Vdc, but total device current is higher than with the 40 Vdc configuration of Circuit A. Thus, since none of the circuits avoided thermal biasing above 200°C and Manufacturer B's devices were susceptable to thermal runaway around 225°C, the life test temperatures were selected as 175°C, 150°C, and 125°C. Circuit A was selected because it placed maximum rated voltage across the device at the lowest total device current.

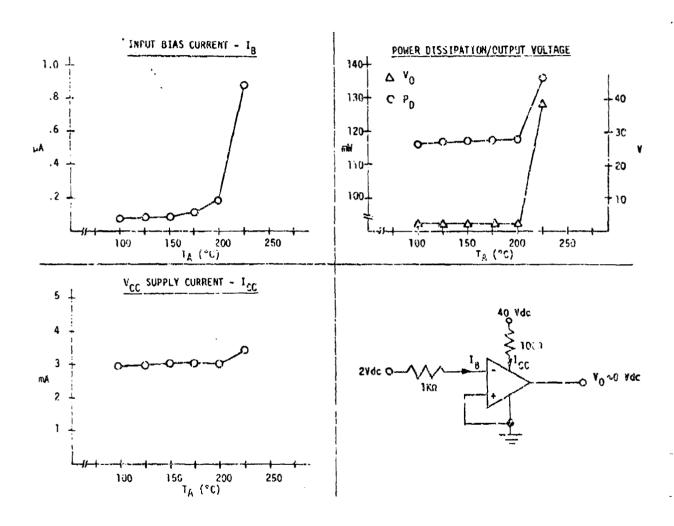


FIGURE D3. MANUFACTURER C MIL-M-38510/10107 (LM118) CIRCUIT EVALUATION

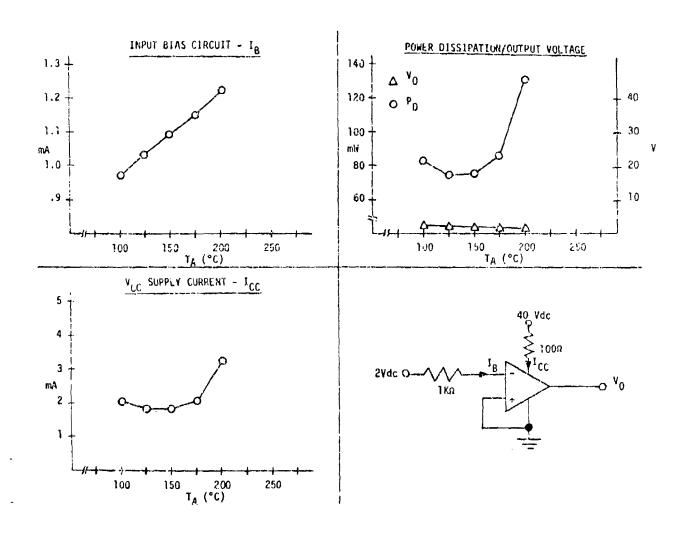


FIGURE D4. MANUFACTURER B MIL-M-36510/10107 (LM118) CIRCUIT EVALUATION

	+2 Voc	+40 Vdc 100%	1 K	+30 Vdc 1002 V0	+2 Vdc •	+20 Vdc 1002 1002 1002 -20 Vdc	
		JIT A PTABLE	CIRCU UNACCE	JIT B P1 4BLE	CIRCUIT (UNACCEPTABLE		
TA (°C)	¹cc (mA)	V _O (VOLTS)	1 _{CC} (mA)	v _O (VOLIS)	I _{SC} (m ^p)	V _O (VOLTS)	
25 125 150 175 200 225 250	2.6 2.4 1.9 2.1 3.2 2.6 A	1.3 1.18 0.81 0.73 8.2 39.55	2.5 2.2 1.5 1.5 1.6 2.2 THERMAL	1.4 1.10 0.80 0.69 0.60 UNSTABLE	7.5 5.3 6.4 6.2 5.8 4.5 THERMAL RUNAWAY	-12.8 -16.7 -18.3 -18.4 -18.5 +10.4	

NOTES: (AVERAGE VALUES FO', DATA FROM BOTH MARUFACTURERS.)

FIGURE D5. MIL-M-38510/10107 (LM118) CANDIDATE BIAS CIRCUITS

 $[\]hat{\mathcal{M}}_{\!\!\!A}$ ONL MANUFACTURER B DEVICE WE IT INTO THERMAL RUMAWAY, AND IS NOT INCLUDED IN THE AVERAGE.

4.0 MIL-M-38510/10201 (723) EVALUATION

Operation of the 723 devices in the MIL-M-38510/10201 accelerated life test bias circuit indicated, as shown in Figures 06 and D7, that the circuit was satisfactory for the Manufacturer D devices, but unsatisfactory for the Manufacturer C devices at life test temperatures above 200°C. The average performance of five Manufacturer D devices exhibited an abrupt 300 mV change in output voltage between 225°C and 250°C. A 300 mV change is not considered excessive. However, the Manufacturer C devices exhibited a 5 Vdc change in output voltage between 200°C and 225°C and a 15 Vdc change between 225°C and 250°C. These changes are considered excessive and the MIL-M-38510/10201 bias circuit was deemed unacceptable at ambient temperatures above 260°C. Attempts to find an alternate circuit configuration that was satisfactory above 200°C were unsuccessful and it was decided that accelerated life tests of the 723 devices should be conducted at ambient temperatures of 200°C, 175°C, and 150°C.

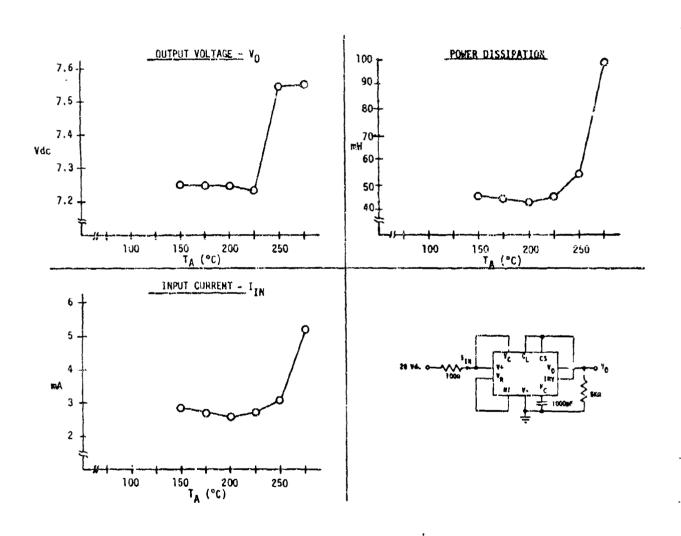


FIGURE D6. MANUFACTURER D MIL-M-38510/10201 (723) CIRCUIT EVALUATION

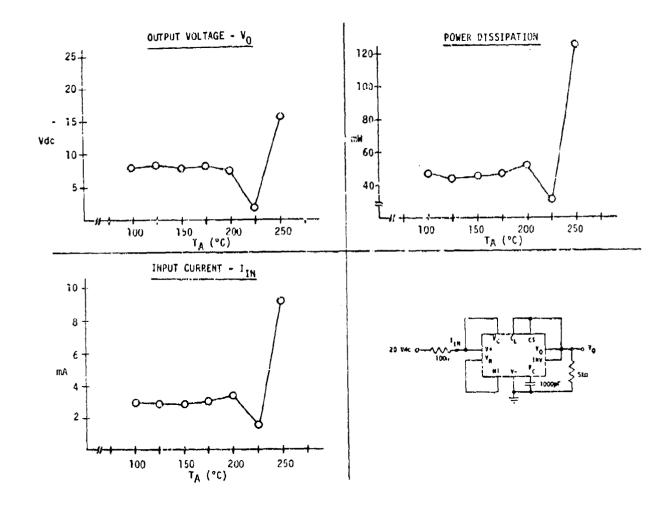


FIGURE D7. MANUFACTURER C MIL-M-38510/10201 (723) CIRCUIT EVALUATION

5.0 MIL-M-38510/10701 (LM109) EVALUATION

Operation of five of each manufacturer's LM109 devices in the MIL-M-38510/10701 accelerated life test bias circuit indicated that the circuit configuration was satisfactory for life testing at ambient temperatures between 260°C and 250°C. Results of the LM109 bias circuit evaluation (average performance of five devices) are shown in Figures C8 and D9, and indicate the devices are in their thermal shutdown mode above 175°C. Although this is not the normal mode of operation, most of the microcircuit junctions, especially the failure prone input transistor junctions, are stressed in a manner similar to normal operation. The output voltage also remains low (%1 Vdc) above 200°C, and the total device current is less than 10 mA. Thus, the circuit meets the established criteria for an accelerated life test circuit at ambient temperatures of 250°C, 225°C, and 200°C.

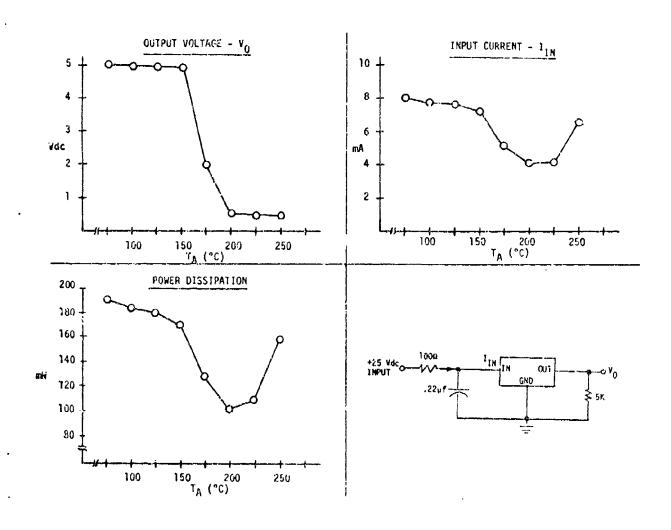


FIGURE DB. MANUFACTURER & MIL-M-38510/10701 (LM109) CIRCUIT EVALUATION

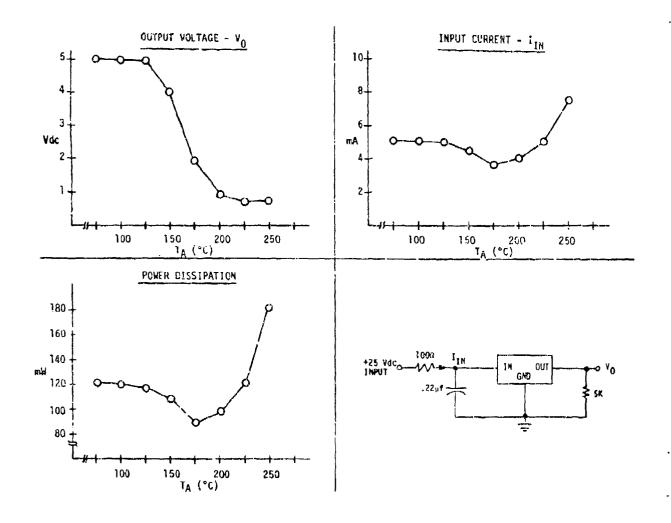
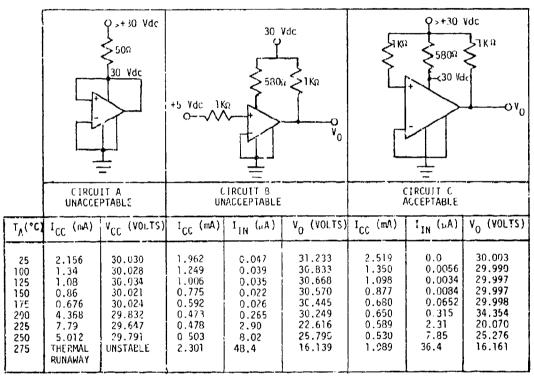


FIGURE D9. MANUFACTURER D MIL-M-38510/10701 (LM109) CIRCUIT EVALUATION

6.0 MIL-M-38510/10304 (LM111) EVALUATION

Operation of LM111 devices in the MIL-M-38510/103A accelerated life test circuit shown as Circuit A of Figure D10 indicated the circuit was not acceptable for use as an accelerated life test circuit. In this circuit the output was tied directly to $V_{\ell\ell}$, which forced the output to a high state and caused the device to draw excessive current at temperatures above 200°C. The circuit was modified, as shown in Circuit B of Figure D10, to current limit the input and output pins. Although this circuit operated acceptably, the circuit was modified at the request of RADC to apply the maximum voltage stress at the inputs. This circuit was evaluted, Circuit C of Figure D10, and operated satisfactorily up to 250°C. The results of the bias circuit evaluation on this circuit are shown in Figures D11 and D12. However, to maintain the output current to a reasonable level if the device should fail with the output in a low state, the resistor tied to the output was changed from 1K to 5K ohms for life testing. The input current was not sufficient to warrant a current limiting resistor; therefore, it was removed from the positive input (pin two) and this input was connected to $V_{\rm CC}$ at pin eight. The final life test circuit is shown in Figure D13. The life test temperatures were selected to be 250°C, 225°C, and 200°C.



AVERAGE VALUES FOR 5 DEVICES

FIGURE D10. MIL-M-38510/10304 (LM111) CANDIDATE BIAS CIRCUITS

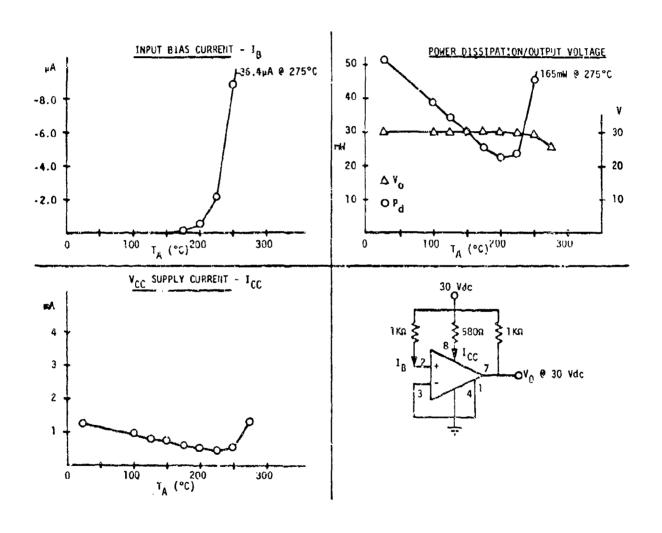


FIGURE DII. MANUFACTURER B M38510/10304 (LMIII) CIRCUIT EVALUATION

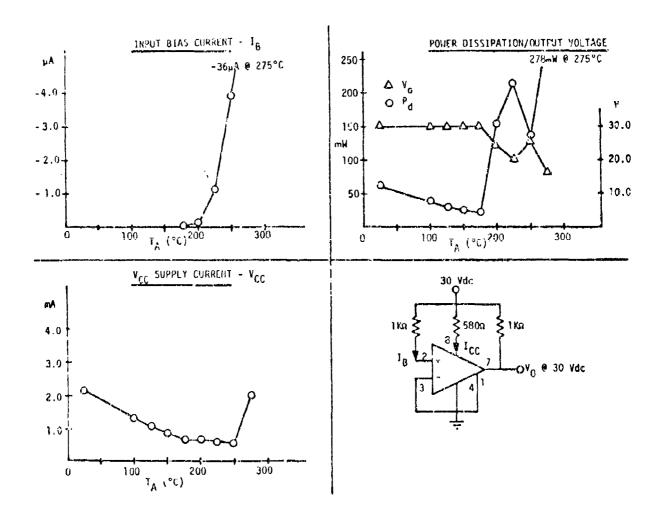


FIGURE D12. MANUFACTURER D M38510/10304 (LM)11) CIRCUIT EVALUATION

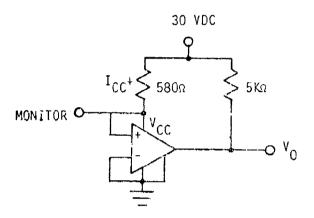


FIGURE D13. M38510/10304 LIFE TEST CIRCUIT

APPENDIX E CHARACTERIZATION TESTS

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3.0	RESULTS OF TRANSFER CHARACTERISTIC STUDY	E13
4.0	REFERENCES	E48

1.0 INTRODUCTION

Characterization tests were performed to supplement the device electrical performance information obtained during initial electrical testing. The characterization testing was performed on a sample basis and consisted of two test groups: dynamic testing, and transfer characteristic studies. The dynamic test group consisted of ten of each manufacturer's device type that had passed the initial baseline tests. These devices were subjected to all the MIL-M-38510 Group A tests not performed during baseline testing. Although these devices were tested to the MIL-M-38510 specifications, only one device, the Manufacturer D 723 device, was a JAN qualified device. This may account for the large number of failures noted in the dynamic testing. The transfer characteristic group consisted of two of each manufacturer's device type. The transfer characteristics of these devices were examined under various conditions of temperature, load, voltage and frequency.

2.0 DYNAMIC TEST RESULTS

The results of subjecting ten of each manufacturer's device type in the MIL-M-38510 dynamic test subgroups are contained in the following sections. The dynamic tests subgroups are those contained in the specific revision of MIL-M-38510 shown in Table E1. Subsequent amendments and revisions of the particular MIL-M-38510 documents have revised the limits, and in some cases the conditions for the dynamic subgroups. In most cases, the revisions have widened the limits so that more devices would now pass these tests. The results of subjecting ten of each manufacturer's device type to the MIL-M-38510 dynamic test subgroups are as follows:

2.1 MIL-M-38510/10104 (LM108A)

The results of the dynamic tests for the LM108A device are summarized in Table E2. Five of Manufacturer B's devices failed the transient response overshoot test at 25°C and all ten devices failed at 125°C. Figures E1 and E2 show the transient response curve of a typical good Manufacturer A device and of a failed Manufacturer B device at 125°C. The Manufacturer B device exhibited considerably more ringing and higher overshoot than Manufacturer A's devices. Five of Manufacturer A's devices and two of Manufacturer B's devices also failed the positive slew rate test at -55°C. Two additional Manufacturer A's devices also failed the three Input Offset Current Sensitivity tests at -55°C.

2.2 MIL-M-38510/10107 (LM118)

Table E3 shows the results of the LM.18 dynamic tests. Nine devices from Manufacturer C failed the 25°C and 125°C positive slew rate test. One device of each manufacturer was inadvertently destroyed during the positive slew rate test at 25°C. Also, there were four Manufacturer C failures at -55°C. The minimum for this test was /5V/us. Nine of Manufacturer C's devices also failed the negative slew rate test. Comparison of the two manufacturer's devices as to slew rate indicate that Manufacturer B's devices are faster and have less sensitivity to temperature for this particular test. All Manufacturer C's

TABLE E1. M38510 SPECIFICATION USED FOR DYNAMIC TESTING

MIL-M-38510 SPECIFICATION	REVISION
/101	D - 15 September 1975
/102	A - 10 May 1974
/103	B - 8 March 1977
/107	A - 15 November 1977

TABLE E2. MIL-M-38510/10104 (LM100A) CHARACIERIZATION TEST SUMMARY.

			4			K. Director		
	Semperature Anni		Mark 2 . 7			1.		Units
retressing.	(-1)	rage,	51984	76. Falleo	Medin	2 6	2	
	45	337.0	23.36	O	362.5	13.59	ပ	
massent Response (f.r.)	1 12	332.5	14.39	ပ	366.0	12.20	0	98
	100 100 1	477.5	134.0	0	557.55	56.74 56.74	0	
	25	12.7	2.4	C	40.3	2.3	5	
Overstant	125	22.6	3.5	o	. 6. 	82.	ō	,.
	. 59	9.6	2.8	с.	£ 5,	ى. م.د	0	
(+) 85	25	.133	010	0	37:	E10.	0	
The state of the s	125	131	510.	0	: 223	£10.	o	V/ 145
	- Si	560.	620.	v	0:1	210.	2	
er CV	35	121.	9:0	0	002.	₽1 0°	0	
Oley Maio	52.	.238	. 210.	0	152.	7:3.	•	V/µs
	25-	.124	, n34	د	.128	010.	0	
1	1	529	.967	0	.525	126.	0	3./An
Apple Uliver (-15)''' yoltage Temperature (-15)'''' conception	, Vp	.384	1.157	0	1.184	1.667	o	
			306	-	360	950		
input Offset Avio (+15)/Al Yoltage Temperature	125	6,6	947	. 0	994	1.609	6	הא/יר
Sensitivity	;							
Security Offices	125	.751	277.	•	.470	.920	•	J. / Art
Voltage Temperature	-55	108.	1.004	0	1.036	1.612	0	
Tabut Offset Al.c / 153/AT	125	189	.382	0	.243	.479	0	J. / V O
Current Sensitivity 10 (113)	-55	.938	1.653	2	800.	151.	0	,
Servit Descay	125	062	436	0	- 045	.209	0	047.6
Current Sensitivity 10 (110)	-55	.940	.940	2	.044	.174	0	i.
Imput Offset 61ro carla	125	. 141	904.	0	135	.337	0	3./¥d
		988.	1.784	2	.048	.167	0	
		101	TOTAL FAILED	~	TOTAL FAILED	ATLED	٥	

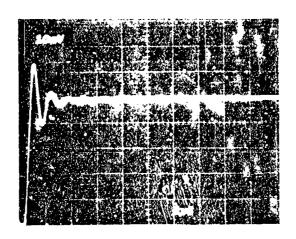


FIGURE 11. TYPICAL CURVE OF NORMAL MANUFACTURER A IM108A TRANSIENT RESPONSE AN 125°C

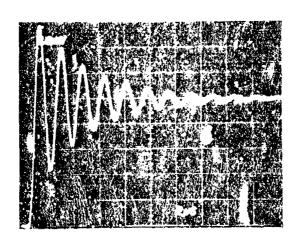


FIGURE E2. CURVE OF MANUFACTURER B LMTOSA FAITING TRANSIENT RESPONSE TEST AT 125°C

TABLE E3. MIL-M-38510/10107 (LM118) CHARACTERIZATION TEST SUMMARY

Parameter		Temperature	L	Manuf. C			Manuf, 8		Unit
***************************************		(·c)	Mean	Sigma	Bo. Falled	Mean	Signua	Faired	ותט
T		25	23,10	0.782	0	17.00	1.000	1 .	
Transfert response	TR(tr)	125	27.00	2.872	ا ہ	20.78	1.641	0	n\$
rise cime	\"'	-55	22.30	1.000	0	16.33	1.000	0	
			1	1.000		10.33	1.000		
		25	6.800	1.398	0	5.0	0.843	0	
Transient reponse	TR(os)	125	13.00	1.944	0	17.60	1.578	0	S
		-55	4,300	0.483	0	500.ټي	0.527	Ü	
		25	59.41	8.608	9	117.2	7.040	0	
Slev rate	SR (+)	125	(0.39	16.26	9	104.9	5.504)	¥/µ
	36 (17	-55	73.18	7.609	•	118.7	6.959	0	
		25	61.44	9.509	1,	75.51	3.064	0	
Slew rate	SR (+)	125	39.08	7.259	9	51.43	2.209	č	l
sies race	24 (+)	-55	77.08	8.622	0	81.66	3.765	ů	¥/us
Input offse		125	25.02	3.428	10	6.359	5 009	0	
vultage temperature sensitivity	4410 (-15)/AT	-55	44,43	12.69	10	17.59	9.408	6	μ¥/°
•	Αν	125	25.62	3.234	10	7.258	5.263	0	"A\.
}	44 _{10 (215)} 01	-55	46.68	13.23	10	15.76	10.30	6	M ,
	AV /47	125	25.G2	3,401	10	6.593	5.172	0	۱۹۷°،
	^{TΔ\} (0) ΟΙ ^{ΨΔ}	-55	44.85	12.88	to	17.62	9.558	6	,,,,,
Input offset		125	35.31	11.27	0	28.74	37.16	0	
current temperature sensitivity	AL10 (-15)/AT	-55	. 26.19	293.1	1	35.39	74.35	O	pA/°
•	Δ1 _{10 (<15)} /ΔΤ	125	12.25	16,10	3	40.60	68.77	0	
	a_10 (<12), p.	-53	32.16	41,95	o	45.85	92.02	0	pλ/v
0	43 ₁₀ (0;/47	125	31.17	28.89	0	44,14	55.39	0	-4/6
	310 (0),2,	-\$5	-5.128	142.8	0	40.35	76.58	0	pA/°
		25	385.0	43.96	-	279.0	34.75	0	
Settling tion	ts (+)	125	392.5	102.0	0	932.0	180.€	0	ms.
	4,41	- 55	356.5	24.95	0	256.0	29.23	0	
		25	469.0	17.45	1,	322.5	107.5	0	
•	ts (~)	125	586.4	33.04	c	490.0	149.7	0	ns
		- 55	390.5	20.06	0	292.5	48.15	0	-
			TOTA	L FAILED	10	TOYA	L FAILED	6	

One device of each manifacturer was accidentally electrically damaged in the test setup reducing this sample size to nine (9) devices.

devices also failed the Input Offset Voltage Temperature Sensitivity Test and six of Manufacturer B's devices failed the 25°C to -55°C portions of this test. As can be seen from the data, the offset voltage of Manufacturer C's devices is more than twice as sensitive to temperature as the offset voltage of the other manufacturer's devices.

2.3 MIL-M-38510/10201 (723)

The results of the 723 dynamic tests are shown in Table E4. All of Manufacturer C's devices and four of Manufacturer D's devices failed the Line Transient Response test. The four Manufacturer D failed devices are only slightly out-of-tolerance, while the parameter value of Manufacturer C's failures are an order of magnitude greater than Manufacturer D's failed values.

2.4 MIL-M-38510/10701 (LM109)

The results of the dynamic tests for the LM109 devices are shown in Table E5. One of Manufacturer D's devices failed the Average Temperature Coefficient of Output Voltage test at 25°C to 125°C, and eight failed the same test in the 25°C to -55°C temperature differential. The Manufacturer D failures in the 25°C to -55°C differential test, however, were the results of start-up problems in the -55°C tests. The $V_{\rm OUT}$ test for these devices failed at -55°C due to start-up problems at this temperature. Three of Manufacturer B's devices failed this same test in the 25°C to +125°C temperature differential. Nine of Manufacturer D's devices also failed Ripple Rejection at 125°C and 100 kHz. Two of these devices also failed Ripple Rejection at -55°C and 100 kHz. All Ripple Rejection failed values were only slightly below the 60db minimum limit and except for one failed value all of the values were less than 60-0.5dB. This device subsequently failed both the 125°C and the -55°C Ripple Rejection tests. Also, five of Manufacturer D's devices failed the Load Transient Response test at 25°C and all this manufacturer's devices failed the test at 125°C and -55°C. All of Manufacturer B's devices also failed the -55°C portion of this test. Manufacturer D's devices were very sensitive to load transients. Both manufacturers exhibited sensitivity to load at -55°C.

TABLE E4. MIL-M-38510/10201 (723) CHARACTERIZATION TEST SUMMARY

Paramet	••	Ambient Test Temp.			Manuf. D			Manuf. C		Units
reramet	F r	lest lem	^{ip} .	Mean	Sigma	No. Failed	Mean	Sigma	No.Failed	
Average Temp		125°C		0.006	0.001	0	0.002	0.001	α	*/°c
Coefficient of Output Voltage	(TC _{Vout})	-55°C		9.009	0.001	0	0.006	0.001	0	
Ripple Rejection	(AVIn AVout)	25°C CR	EF= uF	87.23	1.612	0	90.43	2.264	O	dB
	` '	1	EF4 pF	77.85	1.567	0	77.66	4.091	0	
Outpuc Noise	(N_0)	25°C C _R	EF=	2.560	0.640	0	2,270	0.380	ů	иŊ
	` /	25°C CR	EF≖ lµF	42.50	32.90	0	42.40	27.70	0	
Line Transient Response	(AVout)	25°C		1.107	0.180	5	12.70	7.25	10	mV V
Load Transient Response	$\left(\frac{\Delta V_{OUL}}{\Delta I_{L}}\right)$	25°C	*	-0.102	0,004	0	-0.073	0.006	0	<u>m¥</u> m∧
				TOTA	L FAILED	5	TOTAL I	FAILED	10	

TABLE E5. MIL-M-38510/10701 (LM109) CHARACTERIZATION TEST SUMMARY

			Mar	nufactur	er D	Mar	ufactur	er B	
Parameter .		Test Ambient	Mean	Sigma	Number Failed	Mean	Sigma	Number Failed	Units
Average Temperature Coefficient of	У <u>о</u> от Т	125°C	0.59	0.31	1	0.99	0.99	3	mV/°C
Output Voltage	1	-55°C	30.2	23.5	8	0.52	0.14	0	
		25°C 10 Hz	82.7	6.25	0	68.0	0.78	0	
na Janaara	٠,	[78.7	1.47	0	74.0 66.6	0.90 1.20	0	₫B
Ripple Rejection	A ^{OU} L A ^{IV}	125°C 100 kHz	58.8	4.51 0.78	9	65.8	0.56	-0	ав
	* 0U T	-55°C 10 Hz	78,4	5.07	0	66.0	0.78	0	
,		100 kHz	61.6	2.98	2	80.8	0.84	0	
Output Noise	NO	25°C	41.9	1.79	U	27.0	1.05	0	μ٧
Line Transient	v _{out}	25°C	1,72	0.12	0_	0,78	.54	ŋ	
Response	NI ^V	125°C	1.09	0.14	0	1.07	0.12	υ	ឆា\/\
		-55°C	1.95	0.10	0	1.34	1.97	0	
Load Transient	Vour	25°C	1.49	0.73	5	0.52	0.08	0	
Response	I ₁	125°C	1.28	0.03	10	0.79	0.03	С	mV/mA
		-55°(17.4	5.17	10	11.05	3.58	10	
Current Limiting Point	I _{CL}	25°C	93	0.05	Ü	98	0.00	g	٨
Thermal Shutdown Point	^T J(sh)		162.2	3,59	Û	179.0	5.16	0	°C
			TOTAL F	Alled	10	10TAL	FAILED	10	

2.5 MIL-M-38510/10304 (LM)(1)

The results of the LM111 dynamic test results are shown in Table E6. One Manufacturer D device failed the $t_{\rm RHLC}$ test at 25°C. While at 125°C, nine of Manufacturer D's devices and ten of Manufacturer B's devices also failed the $t_{\rm RLHC}$ test. Two additional Manufacturer D device failures occurred at 125°C during the $t_{\rm RLHE}$ tests.

The current MIL-M-38510/10304 (8 March 1977) does not include the emitter response time tests (t_{RLHE} or t_{RHLE}) and the test limits for the 125°C collector response time were expanded. Seven Manufacturer B devices and two Manufacturer D devices would pass the revised t_{RLHC} tests at 125°C.

TABLE E6. MIL-M-38510/10304 (LM111) CHARACTERIZATION TEST SUMMARY

		TEST	MAN	UFACTURE		MAN	UFACTUR	
PARAMETE	ER	AMBIENT	MEAN	SIGMA	NUMBER FAILED	MEAN	SIGMA	NUMBÉR FAILED
RESPONSE TIME (COLLECTOR)	^t RLHC	25°C 125°C -55°C	140.0 637.0 J19.0	16.3 109.0 8.6	0 10 0	259.0 986.0 132.0	50.6 358.0 9.8	1 9 0
	^t RHLC	25°C 125°C -55°C	155.0 259.0 142.0	10.3 41.9 8.9	0 0 0	165.1 244.0 148.0	4.7 13.8 12.6	C 0 0
RESPONSE TIME (EMITTER)	^t RLHE	25°C 125°C -55°C	438.0 1338.0 348.0	25.6 157.0 18.0	0 0 0	367.0 2126.0 275.0	20.8 944.0 16.3	0 2 0
	^t RHLE	25°C 125°C -55°C	840.0 1544.0 571.0	46.4 115.0 39.2	0 0 0	824.0 1942.0 556.0	50.8 126.0 22.7	0 0 0
			TCTAL	FAILED	10	TOTAL	FAILED	10

3.0 TRANSFER CHARACTERISTIC STUDIES

Device transfer characteristics (output voltage as a function of input voltage) were evaluated to determine the device response to variations in temperature, supply voltage, load conditions, and frequency. Transfer functions were obtained by testing two (2) devices from each manufacturer on a curve tracer or test fixture and varying the conditions such as temperature, frequency, load, and supply voltage. For the regulators (MIL-M-38510/19201 and /10701) and the /10104 operational amplifier varying the load conditions had the most dramatic effect. For the /10107 operational amplifier, varying the temperature produced the more notable effects. The LMIII devices were affected by variations in both load and temperature. The specific test conditions for evaluating device transfer characteristics are detailed in lables E7 and E8. The particular effects of varying these test conditions are noted in the following sections:

3.1 MIL-M-38530/10104 (LM108A)

Comparison of the two curves shown in Figure E3 revealed that Manufacturer A's devices exhibited much more linearity than Manufacturer B's devices. Non-linearity is caused by differences in the thermal gradient between the output and each of the input transistors. Manufacturer A's die layout has the input transistors criss-crossed as shown in Figure E4, to equalize the thermal effects.

However, the slope of Manufacturer A's device curve is positive, and not the expected negative slope of an ideal amplifier. This inversion of the stope is caused by thermal feedback [1]. Varying the temperature had very little effect on the linearity of Manufacturer B's devices, as is shown in Figure E5. Varying the load had no measureable effect on Manufacturer A's devices but an increase in load resistance, as shown in Figure F6, did tend to reduce the non-linearity of Manufacturer B's transfe, curve.

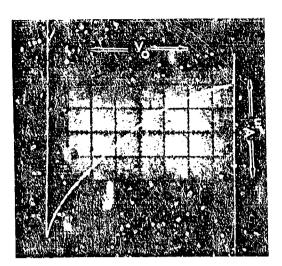
Ideally, an increase in the operating frequency should improve the linearity of the device since effects of thermal gradients are minimized.

TABLE E7. OPERATIONAL AMPLIFIER/COMPARATOR TEST CONDITIONS

]		TEST COND	TTIONS	
DEVICE TYPE	TEST NUMBER	AMBIENT TEMP. (°C)	LUAD RESISTANCE (ahm)	FREQ (Hz)	POWER SUPPLY (Vdc)	COMMON MODE (Vdc)
LM109A	1	25	20K	0.1	+20.0	ນ.0
	2	-55	20K	0.1	<u>+</u> 20.0	0.0
<u> </u>	3	125	20K	0.1	<u>+</u> 20.0	0.0
	4	25	10K	0.1	<u>+</u> 20.0	0.0
	5	25	5 0K	0.1	<u>+</u> 20.0	0.0
	6	25	20K	4,9	<u>+</u> 20.0	0.0
	7	25	20 1.	0.1	<u>+</u> 12.5	۸.٥
	8	25	20r	0.)	<u>+</u> 5.0	0.0
	9	25	20K	0.1	+20.0	+10.0
	10	25	201	0.1	+50.0	-10.0
LM118	1	25	10k	0.1	<u>+</u> 20.0	0.0
	£	-55	70K	0.1	+20.0	0.0
ĺ	3	125	10K	a.1	+20.0	0,0
	÷	25	2K	0.7	+20.0	0.0
	5	25	50K	C-1	<u>÷</u> 20.0	0.0
	6	25	10K	2.0	±20.0	0.0
	7	25	10r.	0.1	+12.5	0.0
	8	25	10%	G.1	± 5.0	6.0
ļ	\$	25	10K	0.1	<u>+</u> 20.0	0.01د
	10	25	10k	0.3	±20.0	-30.0
LM111	1	25	2%.	0.1	+13.0	0.0
	ş	- F9	2 %	2.1	±18.0	0.0
	3	125	2K	0.1	-18.0	6.0
	4	25] 3x	0.1	0.814	0.0
	5	25	10x	0.1	118.0	0.0
	6	25	ξX	3.0	<u>+</u> 15.0	6.0
	7	25	ZX	1.0 ×	±18.0	0.0
]	e	25	ž K	0.1	+12.0	0.0
	9	25	24	0.1	2 6.0	0.0
ļ !	16	75	2×.	0.1	:16.0	+12.0
i	12	25	25	0.1	+38.0	-12-0

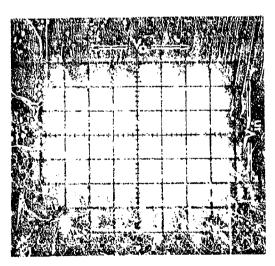
TABLE E8. REGULATOR TEST CONDITIONS

		1	EST CONDIT	IONS
DEVICE TYPE	TEST NUMBER	AMBIENT TEMP.	I _I	FREQ
		(°C)	(mA)	(Hz)
LM109	1	25	5.0	0.1
	2	- 55	5.0	0.1
	3	125	5.0	9-1
	4	25	50 .0	0.1
	5	25	500.0	0.1
	6	25	5.0	10.0
	7	25	5.0	1000.0
723	1	25	1.0	0.1
	2	-55	1.0	0.1
	3	125	1.0	0.1
	4	25	10.0	0.1
	5	25	50.0	0.1
	6	25	1.0	10.0
	7	25	1.0	1000.0



MANUFACTURER A

$$V_{IN} = 2G\mu V/CIV$$
. $V_{O} = 5V/DIV$. $T_{A} = 25^{\circ}C$ $R_{L} = 20k\Omega$ $V_{CC} = \pm 20 \text{ Vdc}$ $V_{CM} = 0 \text{ Vdc}$ Freq. = 0.1 HZ



MANGEACTURER B

FIGURE E3. MIL-M-38510/10104 (MIOSA) TRADSFER CHAPACTERISTIC COCHARISTON

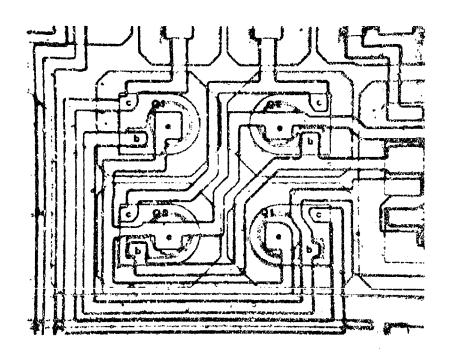
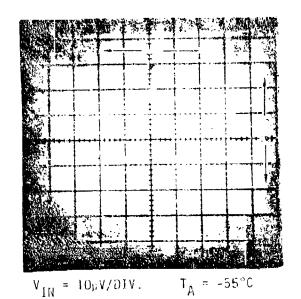
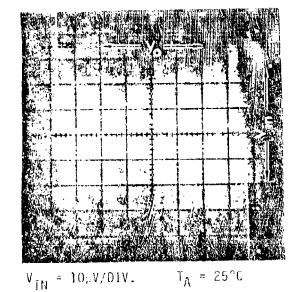
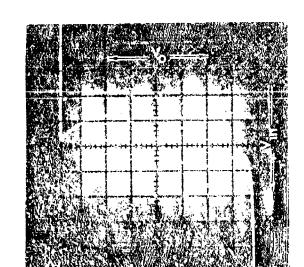


FIGURE E4. MIL-M-38510/10104 (LM108A) MANUFACTUREP A INPUT TRANSISTOR CONFIGURATION







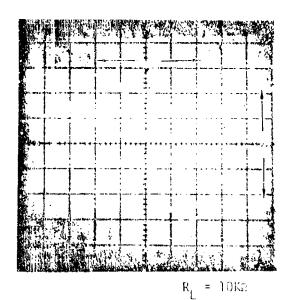
TA = 125°C

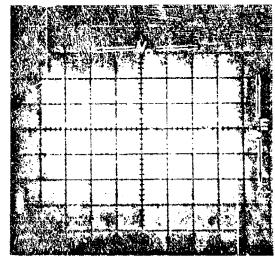
 $R_{L} = 20K\Omega$

 $T_A = A3 \text{ NOTED}$ $V_{G4} = 0 \text{ Vdc}$ $R_1 = 20 \text{K}\Omega$ FREQ = 0.1 HZ

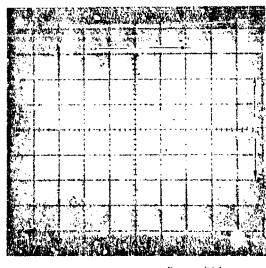
MANOFACTURER B $V_{CC} = \pm 20 \text{ Vdc}$ $V_{CC} = 50/11V$. $V_{14} = 20\mu V/01V$. (UNLUSS NOTED)

FIGURE ES. M38510/10104 (EMESON) TYPICAL TRANSFER CHARACTERISTICS VS. TEMPERATURE





 $R_L = 20 K\Omega$



R_L = 50ks

MANUFACTURER B $v_{CC} = \pm 20 \text{ Vdc}$ $v_0 = 5 \text{V/DIV}$. $v_{IN} = 10 \mu \text{V/DIV}$.

AS ROTED

FEEQ = 6.1 HZ

FIGURE C6. M38510/10104 (LM108A) TYPICAL TRANSFER CHARACTERISTICS VS LOAD

However, attempts to obtain transfer curves at frequencies above 1.0 Hz resulted in excessive hysteresis for both manufacturer's devices, as shown in Figure E7. Thus, our test results were inconclusive as to whether the increased frequency would have an effect on the transfer curves.

Varying the device supply voltage had little effect on the slope or linearity of Manufacturer A's device transfer curves, but decreasing the supply voltage did improve the linearity of Manufacturer B's device transfer curves, as shown in Figure E8. However, decreasing the common mode voltage decreased the slope ($V_{\rm IN}/V_0$) of the transfer curve and also tended to exaggerate any nonlinearities. Figure E9 shows the operation of Manufacturer A's devices under common mode conditions of +10 Vdc, 0 Vdc, and -10 Vdc.

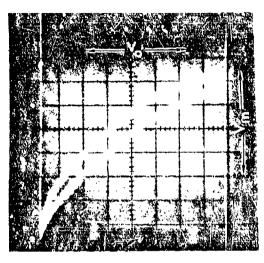
In general, the linearity of the MIL-M-38510/10104 (LM108A) transfer curves was affected by changes in temperature and load. The slope of the LM108A's transfer curve was most affected by changes in common mode voltage.

3.2 MIL-M-38510/10107 (LM118)

Figure E10 shows the difference in linearity between the two manufacturers of the MIL-M-38510/10107 devices. Although the die layout of Manufacturer \dot{c} 's devices is similar to Manufacturer B's layout, the former transfer curve exhibits much less linearity. Temperature had little effect on either the linearity or the slope of the transfer curve for Manufacturer C's devices, as is shown in Figure E11. However, the curves of Figure E12 show that for Manufacturer B's devices, operating them at -55°C tends to decrease the slope of the curve.

Increasing the load resistance slightly increased the slope of Manufacturer B's devices but had little effect on the linearity of the curves. However, increasing the load resistance of Manufacturer C's devices removed most of the non-linearity, as shown in Figure E13.

Variation in power supply voltage and common mode voltage had minimal effect on the linearity of the transfer plats, as is snown in Figures EL4 and



MANUFACTURER A FREQ = 4.0 HZ



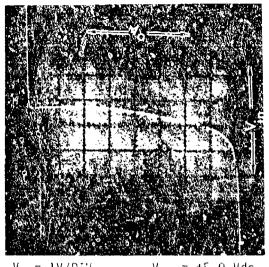
MANUFACTURER B

FREQ = 4 HZ

$$T_{A} = 25^{\circ}C$$
 $R_{L} = 20 \text{ K}\Omega$

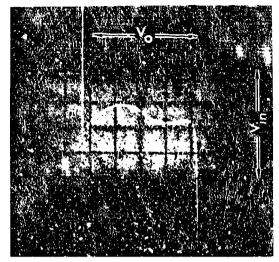
$$V_0 = 5V/D1V.$$
 $V_{1N} = 20\mu V/D1V.$

FIGURE E7. M38510/10104 (LM108A) TYPICAL TRANSFER CHARACTERISTICS VS. FREQUENCY

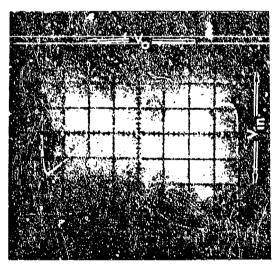


 $V_0 = IV/DIV$.

 $V_{CC} = \pm 5.0 \text{ Vdc}$



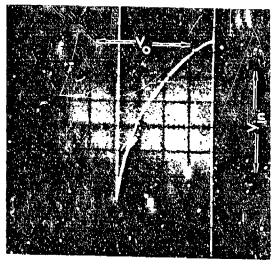
 $V_{CC} = \pm 12.5 \text{ Vdc}$



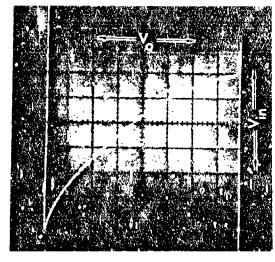
 $V_{CC} = \pm 20 \text{ Vdc}$

$$V_{cm} = 0 \text{ Vdc}$$

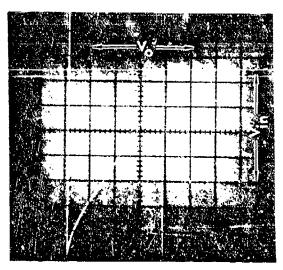
FIGURE 63. M38510/10104 (EM108A) TYPICA: RANSEER CHARACTERISTICS VS. SUPPLY VOLTAGE



 $V_{CC} = +50V/-10V$ $V_{CM} = -10 \text{ Vdc}$



$$V_{CC} = \pm 20V$$
 $V_{CM} = 0 \text{ Vdc}$
 $V_0 = 5V/DIV$.



 $V_{CC} = 10V/-30V$

$$V_{CM} = +10 \text{ Vdc}$$

MANUFACTURER A

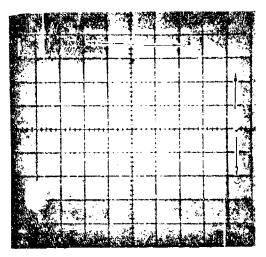
T_A = 25°C

 $R_L = 20K\Omega$ FREQ = 0.1 HZ

 V_{CC} AS NOTED $V_{O} = 10V/DIV$. (UNLESS NOTED)

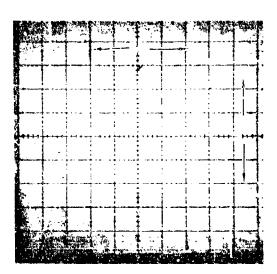
 $V_{IN} = 20\mu V/DIV$.

F1GURE E9. M38510/10104 (LM108A) TYPICAL TRANSFER CHARACTERISTICS VS. COMMON MODE VOLTAGE



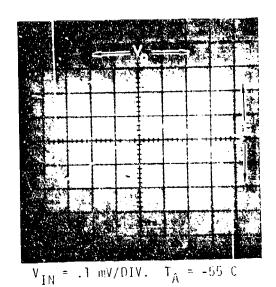
MANUFACTURER B

$$V_{IN} = 50 \text{nV/div}.$$
 $V_0 = 5 \text{V/div}.$ $T_A = 25 \text{°C}$ $R_L = 10 \text{k}$ $V_{CC} = \pm 20 \text{ Vdc}$ $V_{CM} = 0 \text{ Vdc}$ Freq. = 0.1 HZ

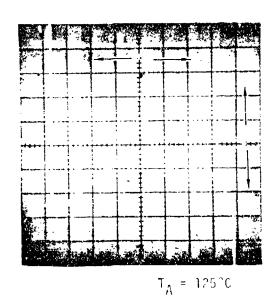


MANUFACTURER C

FIGURE E10. MIL-M-38510/10107 (EMITS) COMPARISON OF TRANSFER PLOTS

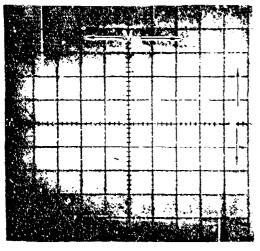


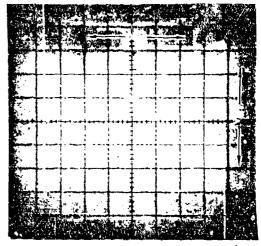
 $T_A = 25^{\circ}C$



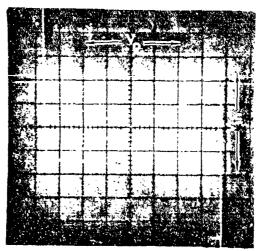
$$V_{CC} = \pm 20 \text{ Vdc}$$
 $V_0 = 5V/DIV.$
 $V_{CM} = 0.0 \text{ Vdc}$ $V_{IN} = 50 \text{ pV/DIV}.$
FREQ C.1 HZ (UNLESS NOTED)

FIGURE E11. M38510/10107 (EM113) TYPICAL MANUFACTURER C TRANSFER CHARACTERISTICS
VS. TEMPERATURE





$$V_{1N} = 50i V/DIV.$$



 $T_{\Lambda} = 125 \text{ C}$

$$V_{CC} = +20 \text{ Vdc}$$

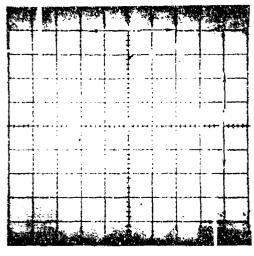
$$V_0 = 5V/DIV$$
.

$$I_A$$
 AS NOTED $V_{CM} = 0 \text{ Vdc}$

$$\Lambda^{CW} = 0 \Lambda qc$$

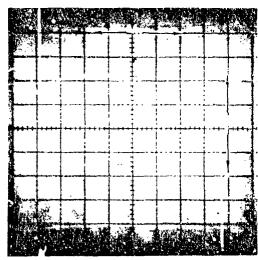
 $R_{L} = 10 \text{K}\Omega$ FREQ = 0.1 H/

EIGURE E12. M38510/10107 (LMT18) LYPICAL MANUFACTURER B TRANSFER CHARACTERISTICS VS. TLMPERATURE



 $R_{\Gamma} = 5K0$

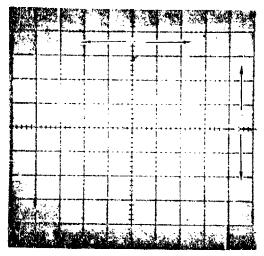
 $R_L = 10K\Omega$



 $R_L = 50K\Omega$

MANUFACTURER B $V_{CC} = \pm 20 \text{ Vdc}$ $V_0 = 5 \text{V/DIV.}$ $T_{\Lambda} = 25 \text{°C}$ $V_{CM} = 0 \text{ Vdc}$ $V_{IN} = 50 \mu \text{V/DIV.}$ R_L AS SHOUN FREQ = 0.1 HZ

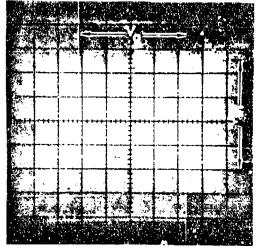
FIGURE El3. M38510/10107 (LM118) TYPICAL TRANSFER CHARACTERISTICS VS. LOAD



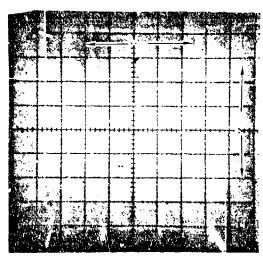
 $V_{O} = 1V/DIV$.

 $V_{CC} = \pm 5 \text{ Vdc}$

$$V_{1N} = 10\mu V/DIV$$
.



 $V_{CC} = \pm 12.5 \text{ Vdc}$



 $V_{CC} = \pm 20 \text{ Vdc}$

MANUFACTURER B

$$R_L = 10 K\Omega$$

$$V_{CM} = 0.0 \text{ Vdc}$$

$$V_{()} = 5V/DIV.$$
 (UNLESS NOTED)

$$V_{IN} = 50\mu V/DIV.$$

FIGURE 114. M38510/1010/ (EMITS) TYPICAL TLANSFER CHARACTERISTICS VS. SUPPLY VOLTAGE

E15. Like the previous operational amplifier, the /10107 devices exhibited excessive hysteresis on the curve tracer at frequencies above 1 Hz, as is shown in Figure E16. Thus, the response of the device to frequency was not determined.

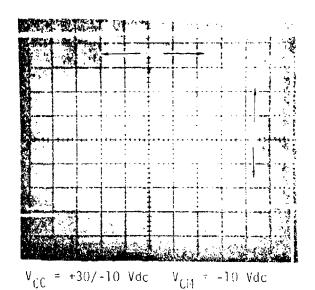
3.3 MIL-M-38510/10201 (723)

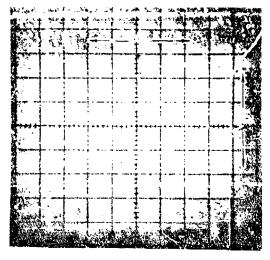
There were no major differences in the transfer plots of both manufacturer's MIL-M-38510/10201 devices. The output of both manufacturer's devices varied only 50 millivolts when the temperature was varied from 125°C to -55°C. However, Manufacturer D's device has small (200 - 300 mV peak-to-peak) oscillation at -55°C. The devices also exhibited very little sensitivity to load, as is shown in Figure E18.

The transfer plots showed considerable hysteresis at frequencies above 5 Hertz. This was found to be directly related, as shown in Figure E19, to the capacitor across the non-inverting input and V-. The transfer plots were run with this capacitor removed and the plots, as shown in Figure E20, showed little sensitivity to frequency other than a slight decrease (.2 - .3 Vdc) in the output voltage at the higher frequencies. In general the MIL-M-38510/10201 devices exhibited very little sensitivity to temperature, load, or frequency.

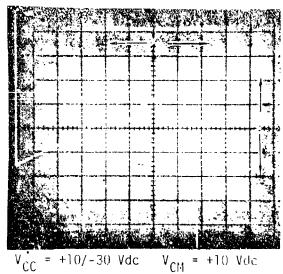
3.4 <u>MIL-M-38510/10701 (LM105)</u>

Manufacturer B's MIL-M-38510/10701 devices exhibited line regulation characteristics with 50 mA of load current similar to those with 5 mA. Also, both manufacturer's devices were relatively insensitive to changes in ambient temperature, as is shown in Figure E21. Subjecting the devices to a constant 500 milliampere load at 25°C without a heat sink induces a sufficient junction temperature rise to cause the devices to go into thermal shutdown.





V_{CC} = ±20.0 Vac $V_{CII} = 0.0 \text{ Vdc}$ $V_{1N}^{(0)} = 50.0791V.$



MANUFACTURER B

TA = 25°C

 $R_L = 10 \text{K}\Omega$

V_{CC} AS NOTED

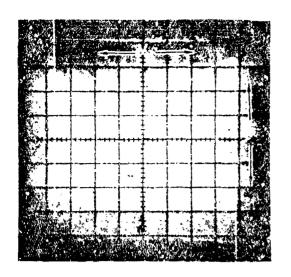
V_{CM} AS NOTED

FREQ = 0.1 HZ

 $V_0 = 5V/DIV$.

 $V_{IN} = 100\mu V/DIV$. (UNLESS NOTED)

FIGURE F15. M38510/10107 (FMTF3) TYPICAL TRANSFER CHARACTERISTICS VS. COMMON MODE VOLTAGE

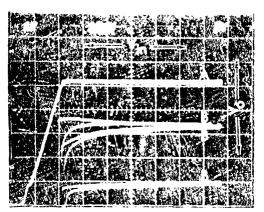


FREQ = 0.1 HZ

FREQ = 2 Hz

TWANDFACTURER B $V_{CC} = \pm 20 \text{ Vdc}$ $V_0 = 5\text{V/DIV},$ $T_A = 25^{\circ}\text{C}$ $V_{CM} = 0.0 \text{ Vdc}$ $V_{IN} = 50\mu\text{V/DIV}.$ $R_L = 10\text{K}\Omega$ FREQ = AS NOTED

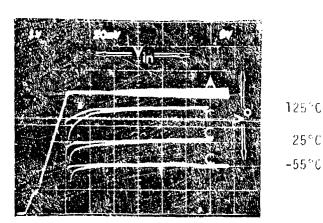
FIGURE E16. M38510/10107 (LM118) TYPICAL TRANSFER CHARACTERISTICS VS. FREQUENCY



125°C 25°C

-55°C

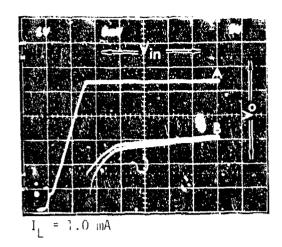
MANUFACTURER C



MANUFACTURER D

 $T_A = AS \text{ NOTED}$ $V_{IN} = 5V/DIV.$ $V_0C = 20mV/DIV.$ $I_L = 1 \text{ mA}$ $V_0A = 1V/DIV.$ FREQ = 0.1 HZ $V_0B = 10mV/DIV.$

FIGURE E17. M38510/10201 (723) TYPICAL TRANSFER CHARACTERISTICS VS. TEMPERATURE





 $1_1 = 10 \text{ mA}$



 $I_{\parallel} = 50 \text{ mA}$

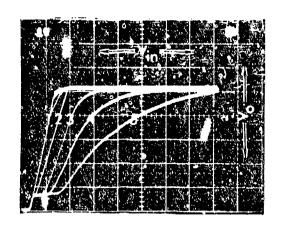
$$I_L$$
 AS NOTED
FREO = 0.1 HZ

$$V_{IN} = 5V/DIV.$$

 $V_{OA} = 1V/DIV.$

MANUFACTURER C
$$I_L$$
 AS NOTED $V_{IN} = 5V/DIV$. $V_0B = 5mV/DIV$. $T_A = 25°C$ FREQ = 0.1 HZ $V_0A = 1V/DIV$. $V_0C = 10mV/DIV$.

FIGURE E18. M38510/10201 (723) TYPICAL TRANSFER CHARACTERISTICS VS. LOAD CURRENT



C _{REF}	OV-40V TRACE	40V-0V TRACE
0μ Г	2	2
1,4 F	3	l
2.5μF	. 4	1
5.0 _ա F	5	1

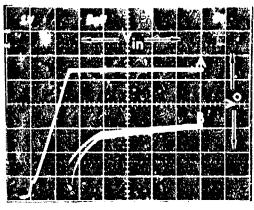
MANUFACTURER C

T_A = 25°C

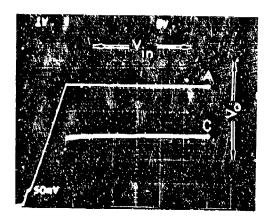
$$V_0 = 1V/DIV$$
.

 $V_0 = 1V/DIV.$ $V_{IN} = 5V/DIV.$

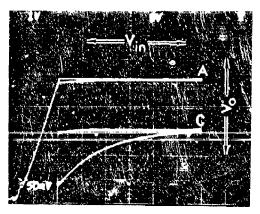
FIGURE E19. M385+0/10201 (723) TRANSFER CHARACTERISTICS VS. C_{REF}



FREQ = 0.1 Hz



FREQ = 10 HZ



FREQ = 1K HZ

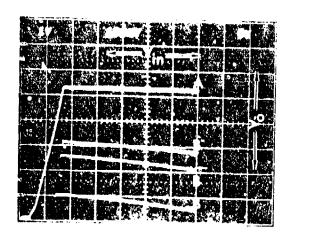
MANUFACTURER C $I_L = 1.0 \text{ mA}$ $T_A = 25^{\circ}C$

FREQ = AS NOTED

 $c_{REF} = o_{H}f$ $v_{O}A = 1V/DIV.$ $v_{1N} = 5V/DIV.$ $v_{O}B = 5mV/DIV.$

 $V_0^C = 50mV/D1V$.

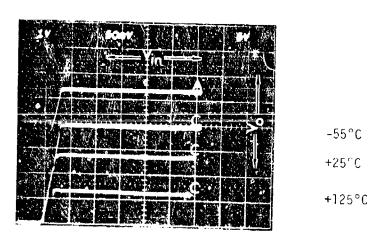
FIGURE E20. M38510/10201 (723) TYPICAL TRANSFER CHARACTERISTICS VS. FREQUENCY



-55°C +25°C

+125°C

MW, JA JURER B



 $V_0^C = 50mV/DIV$.

MANUFACTURER D

TA AS NOTED $I_L = 5.0 \text{mA}$

FREQ = 0.1 HZ

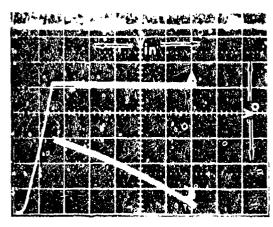
 $V_{IN} = 5V/DIV.$

 $V_0 \Lambda = 1 V/DIV$

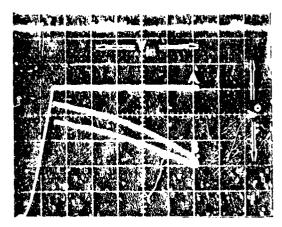
 $A_0 = 100^{10} \text{A} \text{A}$

FIGURE E21. M38510/10701 (LM109) TRANSFER CHARACTERISTICS VS. TEMPERATURE

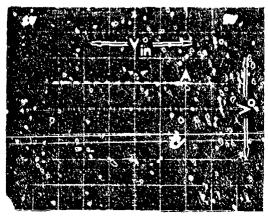
Thus, the devices were subjected to a 300 microsecond 500 milliampere pulsed load at 50% duty cycle. Figure E22 shows that there was minimal deviation in output when the devices were operated at junction temperatures below their rated shut-down temperature. Since the 500 milliampere load curve was made using the pulsed mode of the curve tracer, a magnified curve of the output voltage was not able to be made. The devices also exhibited little senitivity to frequency except that Manufacturer B's device exhibited an increase in line regulation at the 1.0 kHz frequency, as shown in Figure E23. In general, the MIL-M-38510/10701 devices were relatively insensitive to temperature, load, and frequency with the restriction that the load duty cycle does not cause the junction temperature to exceed the thermal shut-down temperature.



 $I_{\parallel} = 5.0 \text{ mA}$



 $A_{\rm H} = 50.0 \, \text{mA}$

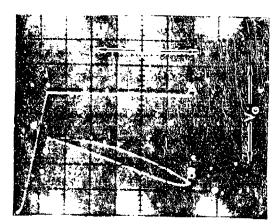


 $I_{\xi} = 500.0 \text{ mA}$ V_{IN} (SEE BELOW)

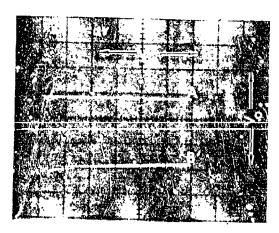
MANUFACTURER B I_L AS NOTED V_{1N} PULSE WIDTH = $300\mu SEC$ T_A = 25 °C FREQ = 0.1 HZ PULSE AMP = 0-35 Vdc $V_0 A = 1V/DIV$, $V_0 B = 20mV/DIV$.

FIGURE 122. M33510/10701 (EM109) TYPICAL TRANSFER CHARACTERISTICS VS. LOAD CIRCUIT

FREQ = 0.1 HZ



FREQ = 10.0 HZ



FREQ = 1.0K HZ

MARUEACTURER B

 $T_{\Lambda} = 25^{\circ}C$

 $T_{L} = 5.0 \text{ mA}$ $V_{TR} = 5 \text{V/DIV}.$ $V_{QB} = 20 \text{mV/DIV}.$ TREQ = AS NOTED $V_{C}\Lambda = 1 \text{V/DIV}.$

LIGURE 123. M38510/10701 (LEMOS) TYPICAL TRANSFER CHARACTERISTICS VS. FREQUENCY

3.5 MIL-M-38510/10304 (LM111)

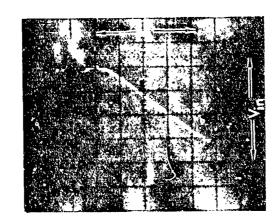
The MIL-M-38510/10304 transfer characteristics were performed for the collector (pin seven) output only and a comparison of Manufacturer B's and D's devices is shown in Figure E24. Varying the temperature degraded the linearity of Manufacturer B's devices as shown in Figure E25. At an ambient temperature of -55°C the slope of the transfer curve increased while at 125°C the slope of the curve is distorted. Temperature variations improved the linearity of Manufacturer D's device transfer curves as shown in Figure E26. The slope of the curves also increased as the temperature increased from -55°C to +125°C.

Similar results were noted in both manufacturer's devices when changes were made in the device load conditions as shown in Figures E27 and E28. A load resistance of 10K ohms in each case provided the best linearity and only slight differences were noted between the 1K ohm load and 2K ohms load curves.

Figure E29 shows the effects caused by varying the input frequency of Manufacturer D's devices. These results are inconclusive since the effects may have been related to the test fixture and not to the device under test. Manufacturer B's devices exhibited similar curves at frequencies of 1.0 Hz and 1.0 kHz.

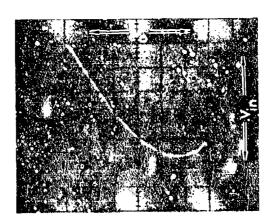
Variations in the supply voltage had no effect on the linearity or slope of either manufacturer's device transfer curves. Changing the common mode voltage of Manufacturer B's devices likewise had no effect on the transfer curves. However, the linearity improved on both common mode voltage transfer curves (+12 Vdc) for Manufacturer D's devices as shown in Figure E30.

The MIL-M-38510/10304 is most affected by changes in ambient temperature and load resistance. For Manufacturer D's devices, optimum performance is provided by reducing the ambient temperature or by increasing the load resistance. Manufacturer B's devices are adversely affected by either temperature extreme; however, at an ambient temperature of 25°C and load resistance of 10K ohms, Manufacturer B's devices provided an optimum transfer curve.



MANUFACTURER B

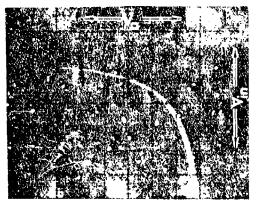
$$V_{III} = 20 \mu V/DIV$$
. $V_{0} = 5V/DIV$. $T_{A} = 25 \text{ °C}$ $R_{L} = 2 \text{ k}$. $V_{CC} = \pm 18 \text{ Vdc}$ $V_{CM} = 0 \text{ Vdc}$ FREQ = 0.1 HZ



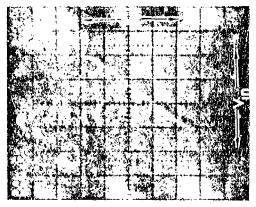
MANULACTURER D

 $V_{III} = 50 \mu V/DIV$

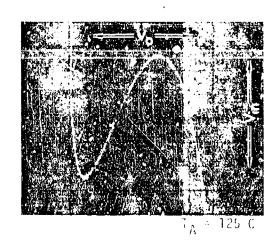
FIGURE 124. MIL-M-38510/10304 (LM111) TRANSFER CHARACTERISTIC COMPARISON



 $V_{\rm BH} \approx 200^{\circ}$. V/61V.



T₁₁ = 25 C



MANUFACTURER B

$$T_{A} = AS MOTED$$

 $R_{L} = 2 K$

V_{CC} = +18 Vdc

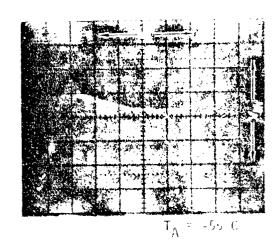
 $V_{CM} = 0 \text{ Vdc}$

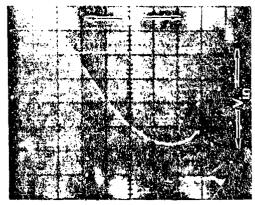
[REQ 0.1 HZ

 $v_0 = 5V/DIV$.

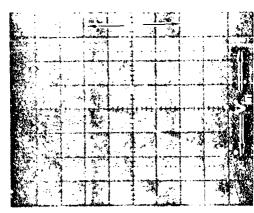
V_{IN} = 20 pV/DIV. (UNLESS NOTED)

FIGURE 125. M38510/10304 (LMILL) TYPICAL TRANSPER CHARACTERISTICS VS. TEMPERATURE





TA = 25 C



 v_{He}^{-1} 100 eV/DIV. τ_{A} = 125 C

MANUFACTORER D

 $R_{\rm l} = 2 \text{ K}$

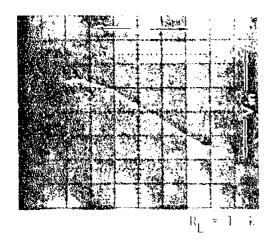
Y_{0.11} = 0 Vdc

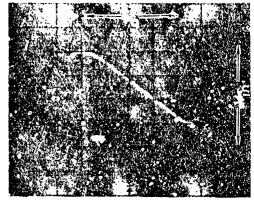
HFQ = 0.1 M

$$V_{G} = 5V/DIV$$
.

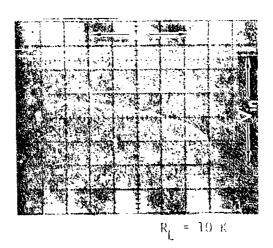
V_{IN} = 50 ..V/DIV. (UNLESS NOTER)

1160R1 126. M28510/10304 (1861) DEPICAL TRANSFER CHARGE PRISTICS VS. 1EMPERATURE





k = 2 K::



MANUFACTURER B

 $T_A = 25^{\circ}C$

R_L AS NOTED

 $V_{CC} = \pm 18 \text{ Vdc}$

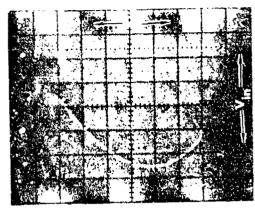
 $V_{Cij} = 0$ Age

FREQ = 0.1 HZ

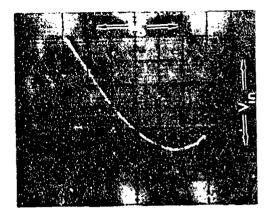
 $V_0 = 5V/DIV$.

 $V_{1N} = 20 \text{ pV/D1V}.$

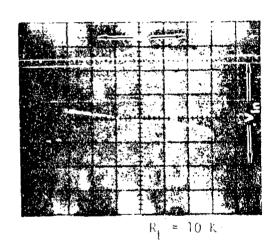
FIGURE E27. M38510/10304 (LM111) TYPICAL TRANSFER CHARACTERISTICS VS. LOAD



R_L = 1 K.



R_L = 2 K.



MANUFACTURER D

T_A = 25°C

RL AS NOTED

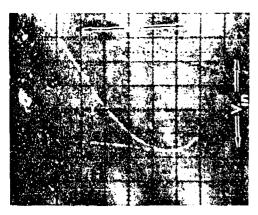
 $v_{CC} = \pm 18 \text{ Vdc}$

 $V_{CM} = 0 \text{ Vdc}$ FREQ = 0.1 HZ

 $V_0 = 5V/DIV$.

 $v_{IN} = 50 \text{ aV/DIV}.$

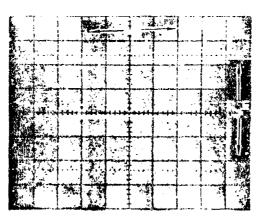
FIGURE L 28. M38510/10304 (LMITT) TYPICAL TRANSFER CHARACTERISTICS VS. LOAD



FREQ = 0.1 H/



FREQ = 1.0 HZ



FREQ = 1.0 kHZ

MANUFACTURER D

$$V_{CC} = \pm 18 \text{ Vdc}$$

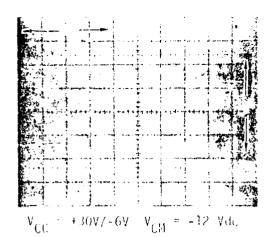
$$V_{CM} = 0 \text{ Vdc}$$

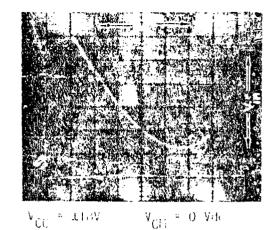
FREQ AS NOTED

$$V_0 = 5V/D1V$$
.

 $V_0 = 5V/D1V.$ $V_{1N} = 50 \text{ pV/D1V}.$

FIGURE 179. MARGIN/10304 (LMILL) TYPICAL TRANSFER CHARACTERISTICS VS. FREQUENCY





V_{CC} = 6V/-50V V_{C11} = +12 Vdc

MARULACTURER D

 $R_{\rm L}^{\prime\prime} + 2.K$

V_{CC} AS NOTED

V_{CII} AS NOTED

FREQ = 0.1 HZ

 $v_0 = 5v/01v$.

 $v_{1N} = 50 . V/DIV.$

figure 1.30. M08510/10304 (FMILL) TYPICAL TRANSFER CHARACTERISTICS VS. COMMON MODE VOLTAGE

4.0 REFERENCES

[1] J. E. Solomon, "The Monolithic OP AMP: A Tutorial Study," IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974.

APPENDIX F

FAILURE ANALYSIS

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1.0 INTRODUCTION

This appendix presents a condensation of the failure analyses performed during the program.

lo facilitate reader use of this appendix, an overview of all failure analysis results is presented in Section 3.0. Individual failure analysis reports are contained in Sections 4.0 through 8.0, and the paragraph numbers for specific reports are cross-referenced in the Section 3.0 overview.

2.0 PROCEDURE

All parts that failed an electrical test during Step Stress and Accelerated Life testing were analyzed to determine the particular failure mode, failure mechanism and probable cause of failure. The general analysis procedure was as follows:

- All failures were retested on the automated microcircuit tester to verify the failure, and to obtain final dc electrical parameter measurements.
- Failed parameters were confirmed using a curve tracer or, if necessary, a bench test set.
- 3) The failure was isolated to a specific junction or element to the extent possible via external pin-pin curve tracer measurements.
- 4) Failures were classified into subgroups (failure categories) on the basis of the analysis findings.
- 5) A representative sample of devices from each subgroup was subjected to a detailed analysis.
- 6) The remaining samples from each subgroup were subjected to the following steps to confirm their categorization and to obtain any additional information:
 - a) Unpowered Bake Each device was subjected to an unpowered bake and retested at 25°C to obtain post bake electrical data. The exact time and temperature of the bake depended on the time and temperature at which the failure occurred. Usually, an overnight bake (16 hours) at the test temperature sufficed.
 - b) Leak Tests Each device was subjected to a helium bomb fine leak test and a fluorocarbon gross leak test.
 - c) Defidding Each device was delidded and subjected to routine optical examinations and documentations.

3.0 FAILURE ANALYSIS OVERVIEW

Summaries of the failure analysis results for each device type are contained in Tables F1 through F5. Each table contains a brief description of each of the different failure symptoms, failure modes, failure mechanisms, causes of device failure, and a paragraph number reference to the related failure analysis report. Certain random failures were not analyzed in detail and are not discussed in the reports, thus no reference paragraph number is listed for them.

TABLE F3-1. MIL-M-38510/10107 (LM118) FAILURE ANALYSIS SUMMARY

C CALLED C MOTOR	QUANTITY OF FAILURES AND TIME OF TAILURE (MOURS) BY TEST CLLL MANUFACTURER B HANDE ACTURER C								F/A
B. FAILUPE MODE					MANUFACTURER C STEP ACCELERATED LIFE				REPOR
C. FAILURE MECHANISM D. CAUGE OF FAILURE	STI.P SIRESS	ACCELERATED LI		13.5	STEP	AUGE	LERATED (1	F E	PARAT
	3,6233	125*6	150°C	175°C	318633	125*(150°C	175°C	MUMBE
A. V _{IO} AND/OR PERR 8. CHANGE: CURRENT FROM RIS TO THE SUBSTRATE C. INVERSION OF THE RESISTOR TUB DUE TO CHARGE MIGRATION C. MOBILE 10.55 OR CHARGES IN THE PASSISATION	39175*C 29150*C	5.64 9.68 3.61.5 2.432 1.664 2.61.28	1561 587 364 168 1664 1*81000	2281 182 184 1916 181000					4.
A. 1:0 H Y _{CM} = -15Y B. V+ 10 IMPUT CHARMEL CURPENT C. PPOBLECT INVERSION OF THE C-H JUNCTION OF THE IMPUT TRANSISTOR D. MOBILE IORS IN THE PASSIMATION			381000 1*≇10G8			164000		164	4.
A. I TO OR THE B. LOW GAIN IN INPUT TRANSISTOR C. PPOBABL: DEFLETION OF THE BASE D. MOBILE JONS OR CHARGES IN THE PASSIVATION				1%:28 1#1009		16) 294000		182000	4.
A. Y ₁₀ CATCHID UP B. MILTED STRIPES AND SHORTED SUBCTIONS C. PARABLY TRENTAL RUHANAY OF CI D. DRYNOM					18200°C 18250°C 28275°C			191 2 9 4000	4.
A. V ₁₀ PITTED TO B. SHORTED CAPACITIES C. DIFFERING BREWLOOMN D. SEFECT IN DIFFECTRIC STO ₂						19128	1 44 1920-00	294000	4.
A. V _{IO} LATCRED UT B. OPEN STREPE OR SMORTED JULICITION C. ELECTRICAL OVERSTRESS D. TEST ERROR		194	Ì	 		191000	1*@^000		4.
RANDUM FAILURES-NUT MIALY/ED IN DETAIL									
A. V ₁₀ AND PSRP (REC-VERED PPOH DELTOCKING)								1954	
A. P. B. HONI C. MONE U. TEST FREOP (INITIALLY PAILED)		4*01000	2#1 1*01000						

TABLE F3-2. MIL-M-38510/10104 (LM108A) FAILURE ANALYSIS SUMMARY

	FAILED PARAMETERS OR SYMPTOMS	·			TIME OF F	r				1/4
B. FAILURE MECHANISM			HANUF ACTU			M		REPORT		
	FAILURE MECHANISM	57EP			IFE.	STEP	ACCELERATED LIFE			PARAG.
D. 	D. CAUSE OF FAILURE	STRESS	175°C	200°C	225°C	STRESS	175°C	200°€	225°C	NUMBER
	Y ₁₀ AND/OR A _{VS}	1#125°C	i	1484	18 84					5.1
в.	CHANNEL CURRENT FROM R7 TO THE SUBSTRATE	19175°C	102	3(48	1648		1			
,	INVERSION OF THE R7 RESISTOR TUB	19225°C	. ₹ 6 4	2 0 64 20128	1016 1064			1	1	
	MOBILE IONS OR CHARGES IN THE	16273	1916	391000	3#128			1		
٠.	PASSIVATION		36500	3*#1000	13250				Ì	
		İ	461000		28500	ŀ				
			1*81000		201000		,	 		i
۸.	V ₁₀ CLICHED NP	-	1				105000	19256	166	5.2
	MELTED STRIPES AND SHORTED JUNCTIONS		Ì	ł			202000	49500	3964	
ί.	THERMAL RUNAWAY AT Q6	2		1			464000	491000	39128	
D.). UNKNOWN		Ì	i				192000	19256	
		1	}	}			}	364000	18500	
		1	Ì		1	l		ŀ	301000	
			1			i	Ì	Į	202000	
			ļ	ļ . <u> </u>			 ├─ <i>─</i>		364000	
	∿ s				}		101	16500	201000	5.3
	NOT DETERMINED (RECOVERED)			1		ì	108	ì	102000	
	SURFACE INSTABILITY	ļ	1	İ			561000		●1€4000	
Đ. ——	PRUBABLY TONIC CONTAMENATION			 			102000			
A,	I IO AND/OR IEB		161	108			192	194	1616	5.4
	PROBABLY DEGRADED INPUT TRANSISTORS	1	19128	10500	1	1	1932	1916	26:58	l i
	PROBABLY CHARGE ACCUMULATION		Ì	ł		į	1064	1864	1	
	TEST ANOMALY (STATIC DISCHARGE) 5°C FAILURES AND RANDOM FAILURES - NOT ANALYZEI	D IN DETAIL	⊥	l		<u> </u>	<u> </u>	<u> </u>	1	
	T C PALLACES AND RANDON PALCORES - HOT WINE 1721	1 0 187	T	1	Ι	<u> </u>	ĭ	1	1	
۸.	V ₁₀ 0 +125°C 0WLY						161000	<u> </u>	164000	
۸.	1 ₁₀ & + 125°C ONLY		<u> </u>						164000	
۸.	1 ₀₅ (-) (RECOVERED WIRN LEFT ON TEST)						166			
***	AL NUMBER OF FAILED PARTS	4	28	29	29	1	17	17	26	

NOTES: * @ +125°C ONLY. ● @ -55°C ONLY.

TABLE F3-3. MIL-M-38510/10701 (LM109) FAILURE ANALYSIS SUMMARY

A. FAILURE MODE	TITKAUP	EST CELL	F/A REPORT				
C. FAILURE MECHANISM	140	ACCELERAT D	MAH	8	PARAG.		
D. LAUSE OF FATEURE	200°C	225°C	250°C	200°C	225°C	250°C	
A. OPEN PIN B. LIFTED WIRE BOND AT THE POST C. KIKKENDALL VOIDING IN AUAI ₂ D. EXCESSIVE AUAI ₂ GROWTH DURING BONDING				16500	1964 194000	18520	6.1
A. OPEN PIN 1 OR 3 B. BRUKEN EXTERNAL LEAD C. MECHANICAL OVERSTRESS D. MISHANDLING		165000			168		6.2
A. OPEN PIN 3 B. BROKEN EXTERNAL LEAD C. AU LEACHING D. TIN SOLDER				194000		10123	
A. al _{sed} [13] 2. NONE C. NOME D. INITIALITY FAILED OR MARGINAL	2.44 1864	1816	294 1916 192000			184000	6.3
RANDUM FAILURES - NOT ANALYZED IN DETAIL		L	 		·		
A. VOUT [4] (UNLY MARGINALLY CAILED)				16500			
TOTAL NUMBER OF FAILED PARTS	1	2	4	3	3	3	

TABLE F3-4. MIL-M-38510/10201 (723) FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE	QUANTITY	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS) BY TEST CELL ACCELERATED LIFE							
C. FAILURE NECHANISH	MAN	~	MAN	C	REPOR'				
D. CAUSE OF FAILUGE	150°C		290°C	150°C	175°C	200°C			
A. I _{SCD} B. MONE						602000	7-1		
C. NUME O. TEST SET DRIFT									
A. V _{REF} OR V _{R LIME} [1] + V _{R LUAD} [4] @ -55°C B. NONE C. NONE						294600	7.2		
D. PROBABLY AN INTERMITTENT TEST SUCKET									
A. I _{OS} B. NOT DETERMINED C. SURFACE INSTABILITY + INITIALLY MARGINAL D. MOBILE CONTAMINANT IONS		194					7.3		
RANDOM FAILURES - NOT ANALYZED IN DETAIL	<u> </u>	نـــــــــــــــــــــــــــــــــــــ		<u> </u>	J	<u> </u>			
A. YR LINE [1] (ONLY MARGINALLY FAILED)		194000							
TOTAL NUMBER OF FAILED PARTS	0	3	0	0	0) <u>a</u>]		

TABLE F3-5. MIL-M-38510/10304 (LM111) FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS) BY TEST CELL								
B. FMILURE MODE	<u> </u>	VANUF ACTUR			MANUS ACTURER D				REPORT
C. FAILURE MECHANISM	STEP	ACCE	LERATED L	IFE .	STEP	ACCELERATED LIFE			PARAG
E. CAUSE OF FAILURE	STRESS	200°C	225°C	250°C	STRESS	200°C	225 ° C	250°C	NUMBE
A. V ₁₀ B. LON P _{FE} IN Q4 C. INVERSION OF THE BASE OF Q4 D. PROBABLY IONIC CONTAMINATION		381000	164 1664 161000		18225°C 18275°C	163 1632 5664 96255 16500 1591000	369 1616 5632 46256 36500 1061000	1 98 3932 79256 10500 20 91000	8.1
A. I ₁₀ B. LOM D _{EE} IN Q2 C. SURFACE INSTABILITY AND BULK-RELATED ME CHARISMS D. FROBABLY IONIL CONTAMINATION	10175°C 20275°C	1	194 1932 4954 29128 69256 58500 281000	364 1816 5832 1864 28128 28256 38500 381000	10200°C	1964	1 e4	198 1 0 500	8.2
A. 1 ₁₈ B. 1046 C. NONE 9. Y _{CM} 700 HEGH	20175°C								8.3
A. 1 _O B. LEURADED Q15 COLLECTOR - SURSTRATE DIOUL C. PROBABLY SEVERSION OF THE COLLECTOR D. PROBABLY CATIC ¹¹ CONTAMINATION		1 0 128		1 64 1 6 8					8.4
+125°C UNLY FAILURES AND RANDOM FAILURES - NOT A	NALYZED IN D	LTAIL							
A. CMR (RETEST OK)						1064	208]
A. A _{VC} (RECOVERED)		10128	1#500						
A. Ayc @ +125°C ONLY		401000		181000					
A. V _{OL} [30]				191000					
TOTAL NUMBER OF FAILED PARTS	5	29	25	24	3	35	29	34	

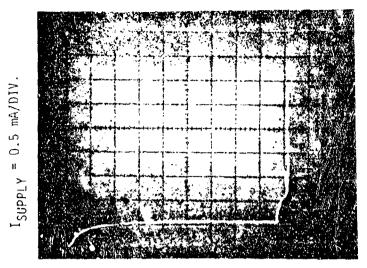
4.0 LM118 FAILURE ANALYSIS REPORT

4.1 RESISTOR TUB INVERSION (MANUFACTURER B ONLY)

Seventy-nine Manufacturer B parts failed ${\rm V_{IO}}$ and/or PSRR during step stress and accelerated life. Ten parts failed ${\rm V_{IO}}$ only, 27 parts failed PSRR only, and 42 parts failed both ${\rm V_{IO}}$ and PSRR. The failures were bake recoverable, indicative of a surface instability mechanism.

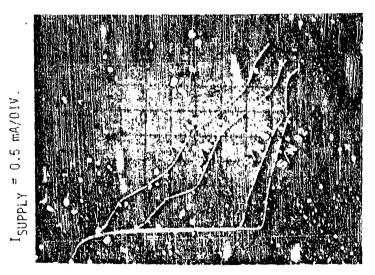
The 52 parts which had failed V_{I0} exhibited excessive V_{I0} at a supply voltage of ± 20 V (V_{CM} = +15, -15V, OV) ranging from -4mV (the specified minimum limit) to -18 mV (latch limit of the test circuit). The failed values were always negative.

 V_{10} was almost always within specification at a supply voltage of ± 5 volts indicating that \mathbf{V}_{10} was supply voltage sensitive. Measurement of V_{IO} (V_{CM} = OV) vs. supply voltage of representative failures disclosed that V_{10} exceeded the limit of -4mV at supply voltages ranging from $\pm 6\text{V}$ to ± 20 V. Below the critical supply voltage, V_{10} was fairly constant and above the critical voltage, V_{10} increased (in the negative direction) rapidly. Since this suggested a possible internal low breakdown/excessive leakage current, the I-V characteristic from V+ (pin 7) to V- (pin 4) of each part was examined on the curve tracer. Each failed part exhibited anomalous leakage from V+ to V- beginning at a voltage proportional to the supply voltage at which V_{10} became excessive. For example, Figure F4-1 shows the I-V characteristic of a normal part, control sample S/N 24, with a V_{IO} (+20V, V_{CM} = OV) of -0.9mV. The characteristic is essentially I_{DSS} of J-FET Q38 amplified by Q7-Q9 until breakdown occurs at 45 volts. S/N's 74, 102 and 61 each had failed V_{TO} after one hour of 175°C life and were found to have critical supply voltages of 6V, 15V and 20V, respectively. The three parts exhibited excessive leakage above V+ to V- equal to 5V, 13V and 33V, respectively, as shown in Figure F4-2. The fourth trace in Figure F4-2 is that of S/N 92 which had normal V_{10} (+.36mV) after four hours at 175°C. V_{10} of S/N 92 would



 V_{SUPPLY} (+ 10 -) = 5 VOLTS/DIV.

FIGURE F4-1. I-V CHARACTERISTIC FROM V+ TO V- OF A GORMAL PART (COGTROL SAMPLE S/N 24)



 $V_{SUPPLY} (+ 10 -) = 5 VOLTS/DIV.$

FIGURE F4-2. 1-V CHARACTERISTIC FROM V+ TO V- OF THEFT VIO TAILURES (S/NS 74, 102 AND 61) AND A PART WITH NORMAL VIO AFTER 518 55 (S/H 90)

not exceed -4mV until the supply voltage was increased to \pm 23 volts and its leakage from V+ to V- became excessive at 37 volts.

The anomalous leakage was traced to channel leakage from resistors R15 and R16 to the substrate (V-). Figure F4-3 shows R15 and R16 of S/N 102 after severing the stripes for isolation. Figure F4-4 shows the leakage from the common contact to R15 and R16 (+) to the substrate (-). This leakage, amplified by Q25, was primarily reponsible for the anomalous current observed between V+ and V-. The pn junction between the resistor diffusion and the n-epi resistor isolation tub and the junction between the tub and the substrate exhibited no leakage and nominal reverse breakdown voltages of 90V and 98V. respectively. This indicated that the leakage from R15/16 to V- was caused by a channel in the tub which extended from the resistors to the substrate due to inversion of the n-type tub. Inversion of n-type material is caused by the accumulation of a net negative charge in or on the passivation layers. To further pin-point the location of the channel, a high potential field effect probe technique [1] was used. A manipulator probe, biased either positively or negatively with respect to the n-tub, was scanned over the region of the tub between the resistor and the substrate isolation diffusion of representative failures (before and after removing the glassivation) while monitoring ${
m V}_{
m TO}$ of the part. It was found that positive potentials of up to 150 volts over any point on the tub did not reverse the inversion and improve V_{10} . This indicated that the width of the anomalous channel was probably much greater than the diameter of the probe and simply could not be totally pinched off with the probe. Negative potential, as low as -75V, would affect V_{TG} . The area of greatest sensitivity was found to be along the outside of resistor R15, between the stripe to the emitter of Q16 and the stripe to the base of Q15 (see Figure F4-3). V_{10} would latch negative at a probe potential of -125 volts above the tub along this area. This is because the negative field enhanced the inversion thereby increasing the conductance of the channel. Negative potential applied above the tub anywhere along the outside of R15 would worsen $V_{1\Omega}$ to some degree which indicated that the channel was distributed along the entire length of RI5. A channel also existed along the

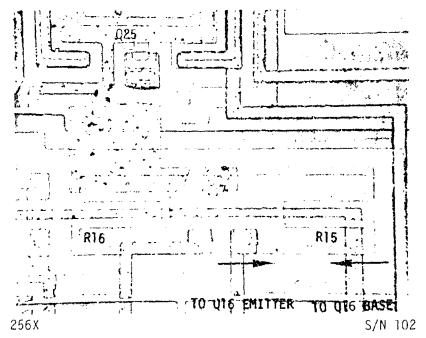
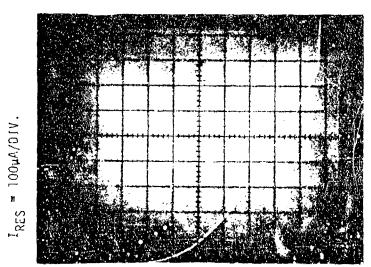


FIGURE F4-3. R15 AND R16 AFTER REMOVAL OF THE GLASSIVATION AND STRIPE SEVERING



V_{RES-SUBST.} = 10 VOLTS/DIV.

FIGURE F4-4. I-V CHARACTERISTIC FROM R15-R16 TO THE SUBSTRATE OF S/N 102

outside of R16, but increasing the inversion with negative probe potential caused ${\rm V}_{10}$ to increase a few millivolts in the positive direction. This indicated that leakage to the substrate from R15 increased ${\rm V}_{10}$ in the negative direction and leakage from R16 increased ${\rm V}_{10}$ in the positive direction. It is suspected that ${\rm V}_{10}$ was always negative at the time of failure because R15 has a greater amount of its perimeter adjacent to the phisolation than does R16. Using the voltage probe it was discovered in the same manner that the n-epi tub containing R12, R13 and R14, shown in Figure F4-5, had also inverted or at least depleted. The exact amount of leakage from these resistors to the substrate could not be determined because other inherent circuit elements existed between the resistors and the substrate that could not be disconnected.

The parts that had failed PSRR only were found to exhibit channel leakage from V+ to V- as did the $\rm V_{10}$ failures, but the leakage was not as severe in the PSRR only failures and usually saturated. Again, this leakage was traced to inversion of the R15-R16 resistor isolation tub. Thus, it is probable that the PSRR failure differed from the $\rm V_{10}$ failures only in degree. This was further substantiated by the fact that any part failing PSRR only, that was left on test, eventually failed $\rm V_{10}$ also.

The resistor tub to substrate junction was reverse biased at 40 Vdc during the tests. Thus, the accumulation of negative charge over the tub was probably the result of separation of mobile ionic species in the fringing field of the reverse biased junction or electron drift in the fringing field along defects in the glass/insulator interface [2]. Microscopic examinations of failed parts disclosed two types of anomalies in the glassivation layer which probably contributed to the failure. One hundred percent of the parts examined (27 out of 27) contained one to three cracks in the glassivation over the wide metalization scripe between Q25 and R15/16, as illustrated in Figure F4-6 and F4-7. Sixty-six percent of the parts (18 out of 27) contained one or more cracks elsewhere on the die, principally over the wide emitter contacts of the PNP transistors and the capacitor electrodes. One hundred percent of

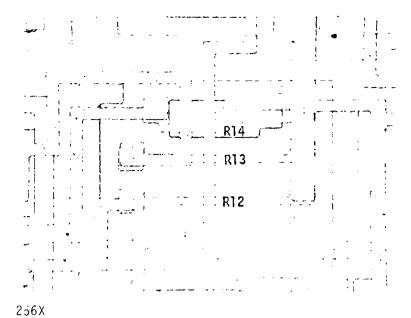
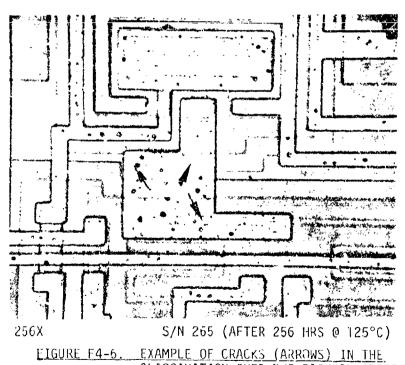
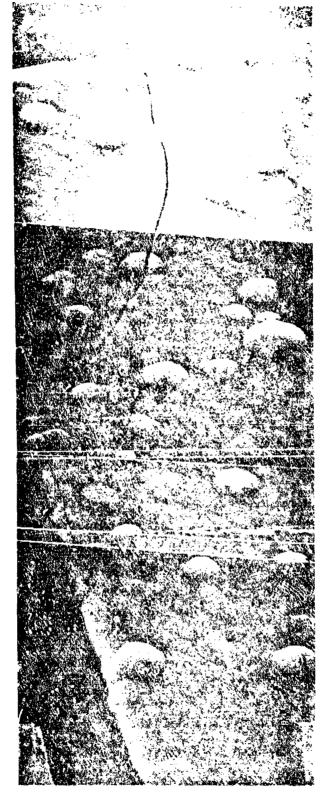


FIGURE F4-5. R12, R13 AND R14 OF THE LM118



EXAMPLE OF CRACKS (ARROWS) IN THE GLASSIVATION OVER THE R15/R16 STRIPE



4500X S/N 293 (STEP STRESS @ 64 HRS/150°C) FIGURE 14-7. SEM PHOTO OF A CRACE IN THE GLASS-IVATION OVER THE RIS/216 STRIPE

the parts also contained pinholes in the glassivation over hillocks in the metalization. As shown in Figure F4-8 and F4-9, the holes appeared to be etched into the glass which indicates that they probably were caused by pinholes in the photo resist during etching of the bonding pad openings. The pinholes were probably caused by flaking of the photo resist over hillocks in the metalization.

4.2 I_{10} ($V_{CM} = -15V$) FAILURE

Four Manufacturer B and two Manufacturer C parts failed I_{10} at a common mode voltage of -15V during accelerated life. The failed values ranged from -592 nA to +143 nA. Three of the Manufacturer B parts also failed + I_{1B} (V_{CM} = -15V) and one of the Manufacturer C parts also failed + I_{1B} (-15V) and - I_{1B} (-15V).

 I_{IO} of five of the parts was excessive at a common mode voltage of -15V because the inverting input bias current (- I_{IB}) was normal, but the non-inverting input bias current (+ I_{IB}) was too low or negative at negative common mode voltages, as illustrated in Figures F4-10 and F4-11. This was indicative of excessive current from V+ to the non-inverting input (pin 3). Examination of the I-V characteristic from V+ to pin 3 (with V- and pin 2 grounded) of each part disclosed the presence of anomalous channel current, as illustrated in Figure F4-12. I_{IO} of the sixth part (Manufacturer C, 125°C failure) was excessive at V_{CM} = -15V because + I_{IB} was excessive and - I_{IB} was negative.

The two Manufacturer C parts recovered prior to bench testing and two of the Manufacturer B parts were baked and both recovered, indicating that the anomalous leakage was caused by a surface related mechanism. The other two Manufacturer B parts were delidded for analysis but both recovered instantly upon delidding and neither contained any visible defects. Thus, the specific failure mode of these parts was not determined. During life test, 38 and 40

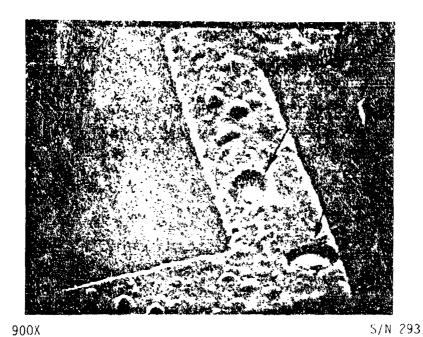
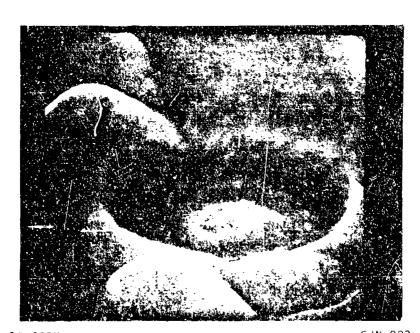


FIGURE F4-8. SEM PHOTO OF TWO PINHOLES (ARROW)
IN THE GLASSIVATION



10,000X S/N 293
FIGURE 14-9. SEM CLOSE-UP DE A GLASSIVATION
PINHOLE

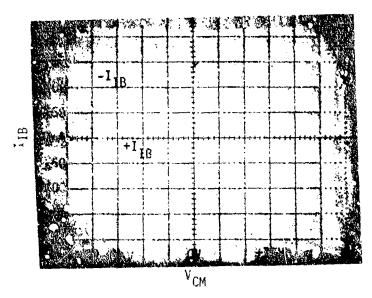


FIGURE F4-10. +IIB_AND -IIB_VS. VCM OF A PART (S/N 174) THAT HAD FAILED 110 DUE TO LOW +IIB AFTER 1.000 HRS AT 150°C

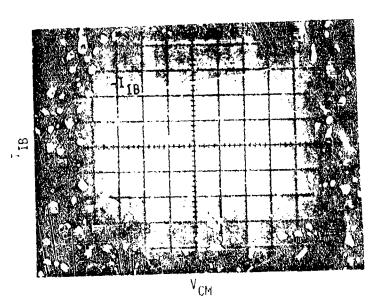


FIGURE F4-11. +I, AMD -I, VS. V_{CM} OF A PART (S)N 144) THAT HAD FAILED IIO DUE TO NEGATIVE ±IIB AFIER 1.000 HOURS AT 150°C

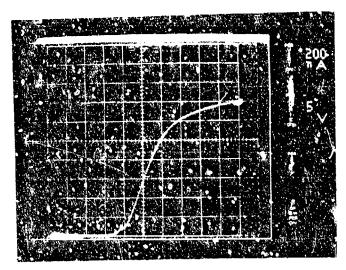


FIGURE F4-12. I-V CHARACTERISTIC FROM V+ TO PIN 3 WITH V- AND PIN 2 GROUNDED OF A PART (S/N 175) THAT HAD FAILED I₁₀ DUE TO NEGATIVE +I_{1B} AFTER 1.000 HRS AT 150°C

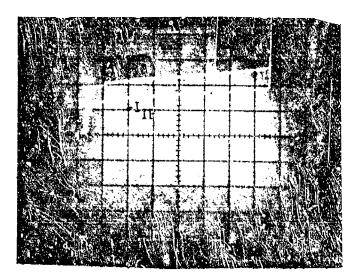


FIGURE 14-13. +1_{IR} AND -I_{IB} VS. V_{CM} OF A PART (S/N 35) THAT HAD FAILED I_{IO} DUL TO EXCESSIVE +I_{IB} AFTER 1,000 HOURS AT 175°C

Vdc was applied from V+ to the inputs. This reversed biased the collector-base junctions of the input transistors. Consequently, it is believed that the anomalous leakage was the result of inversion of the c-b juntion of an input transistor caused by mobile ions or charges in or on a passivation layer.

4.3 I_{10} and/or I_{1B} FAILURE

Two Manufacturer B and four Manufacturer C parts failed combinations of I_{10} and $+I_{18}$ or $-I_{18}$, usually at all three common mode voltages during accelerated life. This was because one of the input bias currents was significantly higher than the other, as illustrated in Figure F4-13. The problem was traced to a gain mismatch in the input transistors. For example, the part illustrated in Figure F4-13 had (at V_{CM} = +15V) an I_{TO} of 75 nA, a + I_{TR} of 246 nA, and a $-I_{13}$ of 173 nA at the time of failure (1000 hours). Die level probing established that, at a V_{CB} of 5 volts and a collector current of 25 μA , h_{FF} of Q3 (the -input transistor) was 83 and h_{FF} of Q4 (the +input transistor) was 52. $+I_{IB}$ was 42% higher than $-I_{IB}$, and h_{FF} of the +input transistor was 37% lower than $h_{\rm FF}$ of the -input transistor, thus, the gain difference accounted for the excessive \mathbf{I}_{10} . The life test data indicated that the gain of both inputs had degraded during life. Initially, $+I_{IB}$ and $-I_{IB}$ at V_{CM} = +15 were 133 and 132 nA, respectively. At the time of failure +I $_{IR}$ was 246 nA and -I $_{IR}$ was 173 nA. The other parts displayed similar degradation except that in one part at the time of failure $-I_{TB}$ was greater than $+I_{TB}$. The gain degradation was present only at low collector currents. The gain of both transistors in the example was 156 at $I_c = 1$ mA. This indicated that the low gain was caused by degradation of the base-emitter junction, probably due to depletion of the p-type base region. I_{IN} and I_{IR} would recover upon baking, indicating that the degradation was the result of a surface related mechanism, probably caused by jonic contamination in the passiviation.

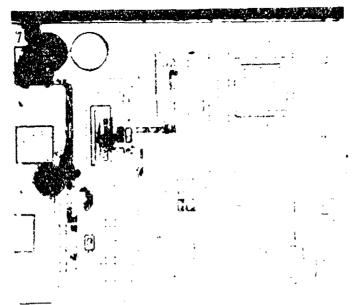
4.4 CATASTROPHIC DAMAGE DUE TO THERMAL RUNAWAY (MANUFACTURER C ONLY)

During step stress, four Manufacturer C parts drew excessive supply current at temperature and failed. The 200°C failure drew nominal current upon reaching temperature, but was drawing excessive current upon completion of the step and was found to be latched up to V- when measured during the post-step parametric tests. Examination of the part disclosed that the V+ wire and the metallization stripes had melted, as shown in Figure F4-14. All of the damage occurred at the V+ ohmic contacts of the circuit elements, and this indicated that the damage was caused by thermal runaway. The other three parts drew excessive current after reaching temperature (250°C or 275°C) and were removed and tested at this point. One part was latched to V+. one part exhibited V_{10} 's of -7mV, and one part failed only -A_{VS} [74]. Examination of these parts disclosed that each contained spears of aluminum extending from a contact of the cross-under (RX1) between V+ and Cl. as illustrated in Figure F4-15, and either spears extending from the ohmic contacts of C1 or a flash-over short across the p-n junction of C1, as illustrated in Figure F4-16, and no other damage. This indicated that the thermal runaway probably initiated at Cl, but the p-n junction contained no apparent defect or deficiency.

The accelerated life test temperatures were limited to 175°C, but three Manufacturer C parts displayed the same failure mode as did the step-stress parts. One part was latched-up after one hour at 175°C and two parts were latched after 4,000 hours at 175°C. As illustrated in Figure F4-17, all three parts contained damage almost identical to that found in the 200°C step-stress failure. The failures indicated that the thermal runaway mechanism was not strictly temperature dependent, but was time dependent as well. However, no reason for the time dependency was found.

4.5 SHORTED CAPACITOR (MANUFACTURER C ONLY)

Five Manufacturer C failures during accelerated life were caused by



105X

S/N 34 (STEP STRESS - 200°C)

FIGURE F4-14. DAMAGE SUSTAINED BY THE 200°C STEP STRESS FAILURE

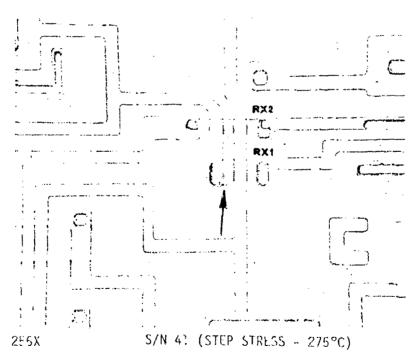
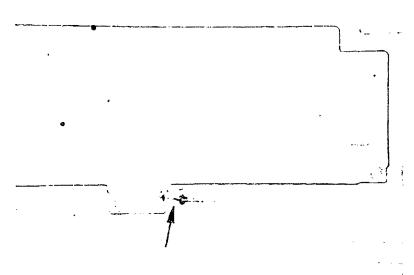


FIGURE F4-15. SPEARS OF ALUMINUM-SILICON (ARROW)
EXTENDING FROM THE CROSS-UNDER
OHMIC CONTACT (GLASS AND ALUMINUM
STRIPES REMOVED)



256X S/N 42 (STEP STRESS - 275°C)

FIGURE F4-16. FLASH-OVER SHORT (ARROW) IN C1
(DELINEATED BY SIRTL ETCH)

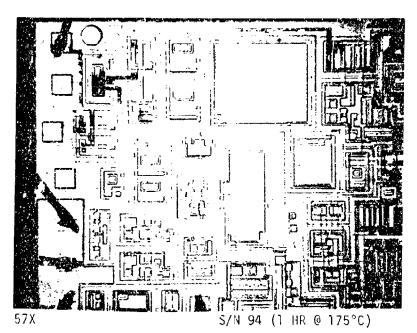


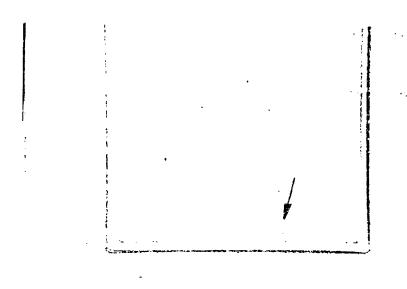
FIGURE F4-17. DAMAGE SUSTAINED BY AN ACCELERATED LIFE TEST FAILURE

defects in the dielectric oxide of one of the MOS capacitors, C2 or C3. Two parts were latched-up to V+, one after 128 hours at 125°C and one after 4,000 hours at 175°C. Examination of the dice revealed no visible damage or defect. In each part, the latch-up was traced to a 40 ohm short-circuit in the MOS capacitor C2. Removal of the aluminum electrode of the 125°C failure disclosed a minute breakdown site in the dielectric at an imperfection in the SiO2, as shown in Figure F4-18. The 175°C failure contained a pinhole defect in the dielectric of C2, as shown in Figure F4-19. Three parts were latched-up to V-, one after four hours at 150°C, one after 2,000 hours at 150°C, and one after 4,000 hours at 175°C. Examination of each die disclosed thermal runaway damage similar to that displayed by parts shown in Figures F4-14 and F4-17. However, die level probing of the capacitors disclosed that in each part, C3 contained a 15-150 ohm short. Removal of the aluminum electrode revealed a pinhole defect in the C3 dielectric of each part, as illustrated in Figures F4-20 and F4-21. Thus it is believed that the thermal runaway in these three parts was initiated by failure of C3 caused by the oxide pinholes.

4.6 CATASTROPHIC DAMAGE DUE TO ELECTRICAL OVERSTRESS

One Manufacturer C part was latched to the positive supply after 1,000 hours at 125°C. Examination of the die revealed that the pin 2 (-input) metalization stripe had vaporized open due to excessive current, as shown in Figure F4-22. A small particle bridged between the pin 2 stripe and the edge of the substrate, but the particle was nonconductive (transparent) and could not have caused the excessive current. Therefore, this failure was probably caused by electrical overstress of pin 2.

One Manufacturer C part had passed the 25°C parametric tests after 4,000 hours at 150°C, but was latched to the negative supply during the +125°C parametric tests. When bench tested, the part was found to be latched negative at 25°C. Examination of the die revealed flash-cvers through the cross-under in the V+ (pin 7) line, RX1, and the cross-under in the COMP C (pin 8) line,



400X

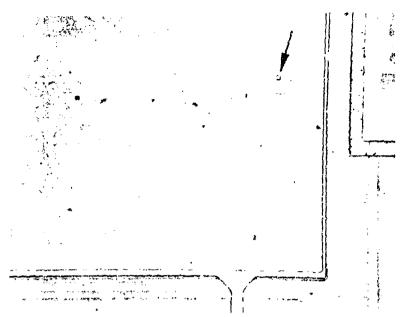
S/N 232 (128 HRS @ 125°C)

FIGURE F4-18. C2 AFTER REMOVAL OF THE ALUMINUM ELECTRODE SHOWING THE BREAKGOWN SITE ARROW)

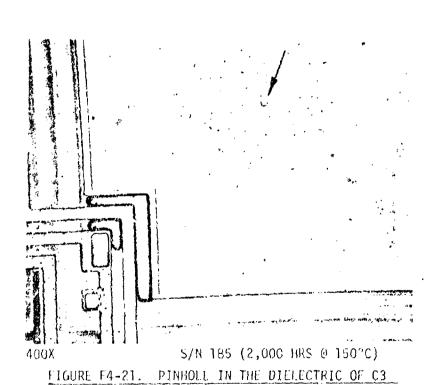
400X

S/N 121 (4,000 HRS @ 175°C)

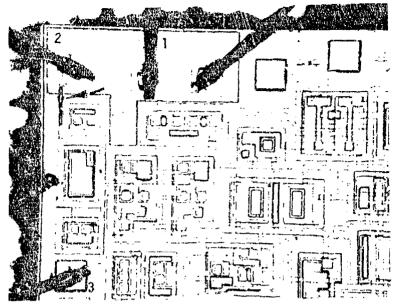
FIGURE F4-19. C2 AFTER REMOVAL OF THE ELECTRODE SHOWING THE OXIDE PINHOLE (ARROW)



256X S/N 132 (4 HRS @ 150°C) FIGURE F4-20. PINHOLE IN THE DIELECTRIC OF C3



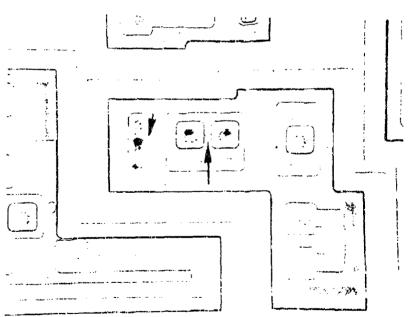
F27



80X

S/N 221 (1,000 HRS @ 125°C)

FIGURE 74-22. MELTED OPEN PIN 2 STRIPE (ARROW)



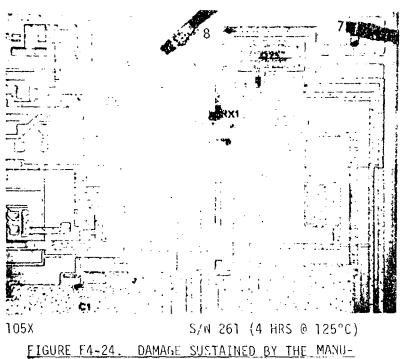
256X

S/N 175 (4,000 HRS @ 150°C)

+ JGURE 14-23. FLASH-OVER DAMAGE (ARROWS) IN Q20 REVEALED BY SIRTL EICH

RX2. Examination of Q20, which is connected between pin 8 and V+, disclosed that it contained flashover shorts, as shown in Figure F4-23. Consequently, this failure was attributed to electrical overstress of Q20 probably caused by a transient or static discharge across pins 7 and 8 prior to the $\pm 125^{\circ}$ C parametric tests.

One Manufacturer B part was latched-up after four hours at 125°C. This part contained damage at Q25, C1 and a cross-under, as shown in Figure F4-24, indicating that it probably had been electrically overstressed.



DAMAGE SUSTAINED BY THE MANU-FACIURER B CATASTROPHIC FAILURE

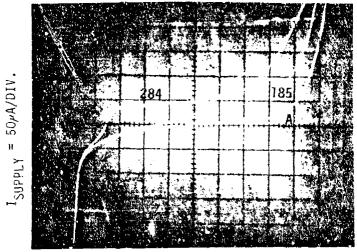
5.0 LM108A FAILURE ANALYSIS REPORT

5.1 RESISTOR TUB INVERSION (MANUFACTURER B ONLY)

Eighty-six Manufacturer B parts failed ${\rm V}_{10}$ and/or ${\rm A}_{\rm VS}$ during stepstress and accelerated life. Sixty-five parts failed ${\rm V}_{10}$, ten parts failed ${\rm A}_{\rm VS}$, and eleven parts failed both ${\rm V}_{10}$ and ${\rm A}_{\rm VS}$. Many of the parts also failed other associated parameters such as ${\rm I}_{10}$, PSRR and CMR because ${\rm V}_{10}$ was severely degraded. The failures were bake recoverable, indicative of a surface instability mechanism.

Of the 75 parts which failed $\rm V_{10}$, the predominant failure was $\rm V_{10}$ at a supply voltage of $\pm 20\rm V$ and $\rm V_{CM}$ of -15V. The failed values were always positive and ranged from 0.5mV (the specified maximum limit) to 19mV (the latch limit of the test circuit). These parts exhibited anomalous current from V+ to V- proportional to the degree of $\rm V_{10}$ failure, as illustrated in Figure F5-1. S/N A is a sample part with normal $\rm V_{10}$. Its I-V characteristic is essentially $\rm I_{DSS}$ of J-FET Q19 amplified by Q22. S/N 185 exhibited a $\rm V_{10}$ of +.63mV after four hours at 225°C and exhibits anomalous current beginning at V+ to V- equal to about 20 volts. S/N 284 exhibited a $\rm V_{10}$ of >19mV after four hours at 225°C and exhibits anomalous current beginning at V+ to V- equal to about 4 volts.

 ${
m V}_{10}$ of these parts would recover instantly upon delidding, as illustrated in Table F5-1. Because the symptoms of these failures were very similar to those of the Manufacturer B LM118 device (reference paragraph 4.1), it was suspected that LM108A failures might also be due to inversion of an n-type resistor tub. To determine if any tub was still slightly inverted or depleted after delidding, a manipulator probe tiased at -100 volts was scanned over the resistor tubs. It was found that the failure, i.e., excessive positive ${
m V}_{10}$, could be reinduced by applying negative potential across the oxide above the tub containing R3, R7, R13, R14 and R30 in the region along the perimeter of R7 adjacent to the isolation diffusion were shown in Figure F5-2. The leakage



 V_{SUPPLY} (+ TO -) = 5 VOLTS/DIV.

FIGURE F5-1. I-V CHARACTERISTICS FROM V+ TO V-OF A NORMAL PART (S/N A) AND OF TWO PARTS THAT HAD FAILED V₁₀ (S/Ns 185 AND 284)

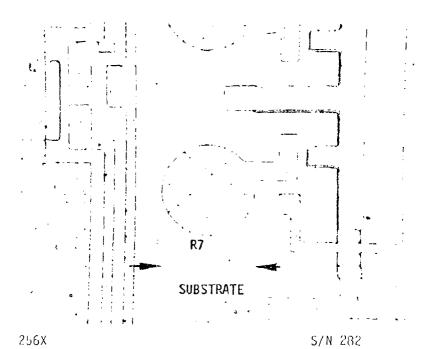


FIGURE F5-2. RESISTOR R7 SHOWING THE REGION OF ANOMALOUS CURRENT (ARROWS)
AS DETERMINED VIA THE VOLTAGE PROBL

TABLE F5-1. EXAMPLES OF VIO RECOVERY DISCLAYED BY THE MANUFACTURER B LM108A UPON DELIDDING

٧	6	٧.,	=	-150	(mV)
. 1()	- 2	100			(,

							17	1/
<u>S/N</u>	CELL	*F	L _R	<u>e to</u>	e t _F	e t _R	PRIOR TO 1/2 DELIDDING	IMMEDIATELY AFTER 1/ DELIDDING
2 82	225°C LIFE	4 HR	4 HR	-0.03	>+19	•	+10	-0.01
141	225°C LIFE	4 HR	1000 ER	+0.05	>+19	>+19	+37	+0.24
62	200°C LIFE	4 HR	1000 HR	-0.20	>+15	+11	+7.2	+0.0\$
202	175°C LIFE	1000 HR	1000 HR	-0.35	>+79	-	+3.2	~0.20

NOTES

 t_F = Time of Failure

t_R = Time of Removal From Life Test

t₀ = Prior to Life Test

1/ = Curve Tracer Test

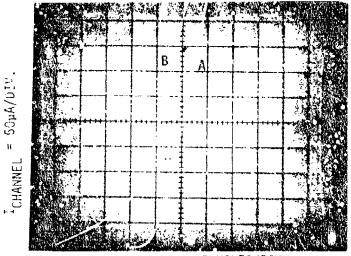
current from the resistors to the substrate (determined after severing appropriate stripes) would increase upon application of the negative field in this region of the tub, as shown in Figure F5-3. This indicated that the failures probably had been caused by anomalous channel current from the resistors to the substrate due to inversion of the n-type resistor tub. Inversion of n-type material is caused by the accumulation of a net negative charge in or on the passivation layers.

The parts that had failed only A_{VS} exhibited two basic types of anomalous gain. Some parts exhibited negative gain that was too low at $V_{OUT}=+15V$ and -15V as illustrated in Figure F5-4 and others exhibited positive gain that was too low at $V_{OUT}=+15V$ as illustrated in Figure F5-5. The gain characteristics indicated that the low gain was probably caused by gain distortion due to variation in V_{IO} with output voltage. These parts exhibited anomalous current from V+ to V-, as illustrated in Figure F5-6 and recovered instantly upon delidding, as shown in Table F5-2. These findings indicate that the failure mode of the parts failing only A_{VS} was probably the same as that of the V_{IO} failures, i.e., inversion of the R7 resistor tub.

The resistor tub to substrate junction was reverse biased at 40 Vdc during the tests. Thus, the accumulation of negative charge over the tub was probably the result of separation of mobile ionic species in the fringing field of the reverse biased junction or electron drift in the field along defects in the glass insulator interface [2]. Microscopic examination of failed parts disclosed anomalies in the glassivation similar to, but not as severe as, those found in the Manufacturer B LM118 failures. Seventy percent of the parts examined (21 out of 30) contained at least one crack in the glassivation, as illustrated in Figure F5-7. Using an aluminum etch it was determined that 30% (10 out of 30) of the parts also contained glassivation pinholes.

5.2 CATASTROPHIC DAMAGE DUE TO THERMAL RUNAWAY (MANUFACTURER A ONLY)

Thirty-seven Manufacturer A parts failed during accelerated life that



V_{RESISTOR} SUBSTRATE = 5 VOLTS/DIV.

FIGURE F5-3. I-V CHAPACTERISTIC FROM R7 TO THE SUBSTRATE WITH NO FIELD (TRACE A)
AND WITH A NEGATIVE FIELD (TPACE B) APPLIED ACROSS THE OXIDE OVER THE TUB

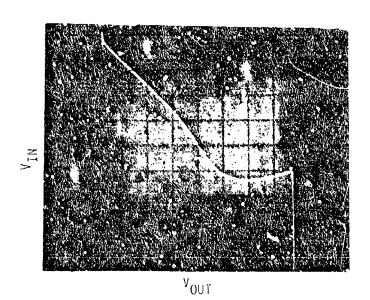


FIGURE 15-4. GAIN CURVE OF A PART WITH LOW

+A_{VS} [71] AND - A_{VS} [72]

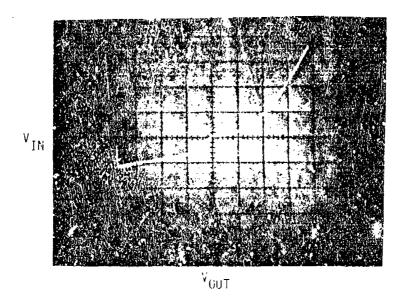
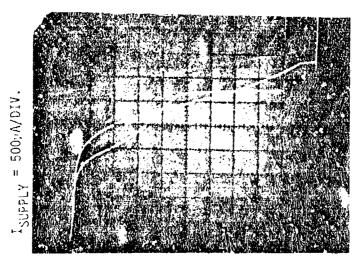


FIGURE F5-5, GAIN CURVE OF A PART WITH LOW +AV5 [7]



 Y_{SUPPLY} (+ TO -) = 5 VOLTS/DIV.

FIGURE F5-6. I-V CHARACHERISTICS FROM V+ TO V-OF TWO PARTS WITH LOW GAIN

TABLE F5-2. EXAMPLES OF AVS RECOVERY DISPLAYED BY THE MANUFACTURER B LM108

UPON DELIDDING

!	IMMEDIATELY <u>!</u> / ATTER <u>DELIDDIMG</u>	375 375	200	750 341 200 100
STORY	17 PRIOR 10 OELIDDING	75 25	원	19 13 13 15 15
PARAMETER HISTORY	e t	¢ 1	•	म् ७ च च
PAR	رخه ا بر	왕 의	S	24 97 177 1754
	e to	361	8£\$	3628 264 530 267
	PARAMETER	+A _{VS} [71] (V/mV) -A _{VC} [72] (V/mV)	+Ays [71] (V/mV)	+A _{VS} [71] (V/mV) -A _{VS} [72] (V/mV) +A _{VS} [75] (V/mV) -A _{VS} [76] (V/mV)
	→ 24	1000 HRS	1000 HRS	1000 HRS
	اند. مرب	1000 HRS	1360 HRS	256 HRS
	פנו	175°C LIFE	200°C LIFE	225°C LIFE
	S/N	235	104	171

NOTES

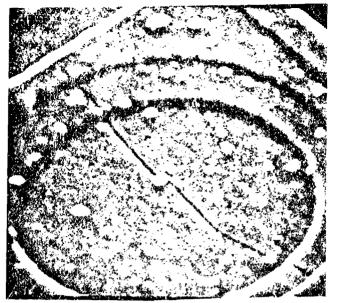
t_F = TIME OF FAILURE

t_R = TIME OF REMOVAL

t_O = PRIOR TO LIFE TEST

1/ = CURVE TRACAER TEST

FAILED PARAMETERS ARE UNDERLIMED.



200X S/N 374

FIGURE F5-7. FXAMPLE OF GLASSIVATION CRACK IN THE MANUFACTURER B LM108A (SEM PHOTO)

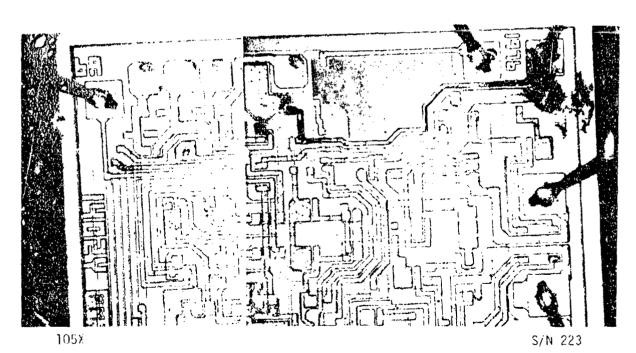


FIGURE F5-8. EXAMPLE OF MOST SEVERE DAMAGE SUSTAINED BY A MANUFACTURER A LMIOSA

were latched to either V+ or V-. Twenty-six parts were date coded 7642, ten parts were date coded 7643, and one part was date coded 7652. Examination of the parts disclosed catastrophic damage such as depleted or melted aluminum along the V+ stripe and aluminum spears protruding from various ohmic contacts to V+. An example of the most severe damage found is shown in Figure F5-8. Some parts contained only depleted aluminum and aluminum spears at the Q6 emitter contact, as illustrated in Figure F5-9. Every failed part, regardless of the amount of total damage present, contained depleted aluminum or spears at the Q6 emitter contact, which indicated that the problem originated at Q6. The life test monitor readings revealed that the failed devices drew excessive current indicating that the failures had occurred while the parts were at elevated temperature, consequently, a thermal runaway mechanism was suspected as the cause rather than any external electrical overstress condition. Furthermore, the life test start-up had indicated that the 7642 date coded parts were susceptible to thermal runaway (Ref: Section 6.1).

Q6 is a lateral PNP transistor. The failed Q6 transistors almost always contained an aluminum-silcon melt-channel or an aluminum spear extending from the emitter contact, indicative of excessive emitter current. The emitter of Q6 is connected directly to V+, but its collector-base is connected to circuitry of sufficient impedance to limit the collector current. However, a lateral parasitic PNP transistor exists between the emitter of Q6 and the substrate. As shown in Figure F5-10, the base current, $I_{\rm g}$, of QC can cause a slight parasitic PNP collector current, \mathbf{I}_{CP} , to flow from the Q6 emitter to V-. At elevated temperature, this current can possibly increase to damaging levels since there is no series limiting resistance for the parasitic current path. The path of damage emanating from the Q6 emitter always pointed in the direction of the c-b contact (the direction of base current flow), as illustrated in Figure F5-11, indicating that the damage probably was the result of excesssive parasitic PNP collector current. Yransistor Q6 is adjacent to three "zappable" transistors, Q29, Q30, and Q31, that are used to trim the offset voltage. However, in many of the failed parts, none of the three transistors had been zapped; therefore, the proximity of Q6 to these transistors was not considered significant.

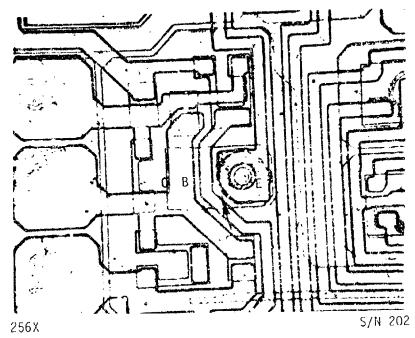


FIGURE F5-9. DEPLETED ALUMINUM AND ALUMINUM SPEAR (ARROW) AT THE Q6 EMITTER

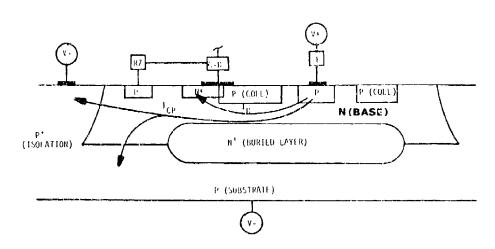


FIGURE F5-10. CROSS-SECTIONAL SKETCH OF Q6

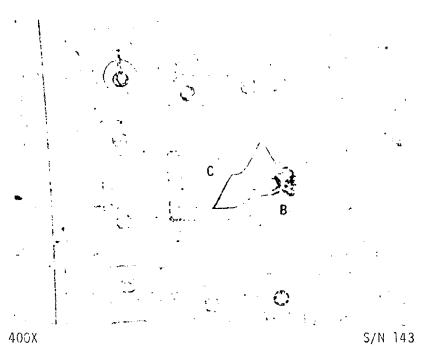


FIGURE F5-11. PATH OF DAMAGE EMANATING FROM THE Q6 EMITTER AS DELINEATED WITH SIRTL ETCH

The failure data showed a time-temperature dependency but the exact cause of the dependency was not established. The failure mechanisms identified in these parts involved parasitic PNP current and localized thermal runaway which led to excessive Q6 emitter current and aluminum melting or migration/silicon dissolution which led to the opens and shorts. The physical appearance of the melting and migration indicated that the damage probably occurred relatively rapidly with little time dependency. Parasitic PNP current and thermal runaway are temperature dependent, but ordinarily are not time dependent mechanisms. Examination of the life test monitor readings disclosed no sign of supply current increase with time in the parts that failed. The supply current of each part was constant until the time of failure at which point the current jumped and the part failed.

5.3 AVS FAILURE DUE TO SURFACE INSTABILITY (MANUFACTURER A ONLY)

Nine Manufacturer A parts failed $+A_{VS}$ [71] during accelerated life. The failed values ranged from 79 to 30 V/mV. All nine parts were left on test. Three parts failed catastrophically at 2000 hours due to thermal runaway at Q6. By 4000 hours, $+A_{VS}$ [71] of the other six parts had recovered as illustrated in Table F5-3. The recovery indicated that the gain failures probably were caused by a surface related mechanism. Since the parts had recovered the exact failure mode could not be determined.

TABLE F5-3. EXAMPLES OF +AVS [71] RECOVERY

VALUE OF +A_{VS} [71] (V/mV)

S/N	CELI. TEMP	FAILURE	INITIAL	<u>1_HR</u>	256 FR	1000 HR	2000 HR	4000 HR
332	175°C	1 HR	163	<u>79</u>	101	142	128	139
194	175°C	1000 HRS	717	6ප0	620	<u>36</u>	<u>23</u>	656
214	175°C	2000 HRS	509	409	402	91	32	104

MOTES

FAILED VALUES ARE UNDERLINED

5.4 I₁₀/I_{IB} FAILURES - TEST ANOMALY

Four Manufacturer B parts and nine Manufacturer A parts failed ${}^{4}I_{IB}$, ${}^{4}I_{IB}$, and/or I_{IO} through 500 hours of accelerated life. During the same time period, three Manufacturer A control parts also failed I_{IO} and ${}^{4}I_{IB}$. All three exhibited excessive ${}^{4}I_{IB}$ and ${}^{4}I_{IB}$ at each common mode voltage and supply voltage. One part was analyzed and found to contain no anomaly. The other two parts were baked for 16 hours at 250°C, and both recovered. The history of ${}^{4}I_{IB}$ and ${}^{4}I_{IB}$ at ${}^{4}V_{CM}=0$ volts and ${}^{4}V={}^{4}20$ volts of each control part is presented in Table F5-4. The accelerated life failures likewise recovered when baked.

In view of the failure of the three control parts, it was suspected that the degradation was caused by the parametric testing or by handling of the parts. Experiments were conducted which established that the parametric testing did not induce any detectable degradation. Therefore, it was decided to treat the LM108As as static sensitive parts and implement all precautionary measures for handling such parts. This was done immediately after the 500 hour test point and, as a result, no further I_{10}/I_{18} failures of this type were encountered. Apparently, the input transistors of the failed parts had been degraded by static charge generated during handling. For reasons unknown, the damage was not permanent and could be annealed by baking.

TABLE F5-4 - IB HISTORY OF THE THREE FAILED MANUFACTURER A CONTROL PARTS

I_{IB} (nanoamperes)

	S/I	191	N/S	62	S/N 63	53
	+I _{IB} (0,20)	"IB (0,20) -1 IB (0,20)	+1 ₁₈ (0,20) -1 ₁₈ (0,20)	-1 ₁₈ (0,20)	+I ₁₈ (3,20)	+1 ₁₈ (0,20) -1 ₁₈ (0,20)
INITIAL VALUE (3/24/77)	90.706	0.683	0.997	1.050	0.695	0.682
VALUE PRIOR TO FAILURE (10/5/77)	0.766	0.740	1.116	1.082	0.743	0.733
VALUE AT THE TIME OF FAILURE (10/11/77)*	* 8.2	8.5	14.0	13.9	8.0	8.5
VALUE AFTER BAKING	1.100	1.073	•	•	1.157	1.158

* VALUE OBTATNED DURING BENCH TEST © DELIDDED FOR F/A

6.0 LM109 FAILURE ANALYSIS REPORT

6.1 OPEN PIN DUE TO INTERMETALLIC GROWTH (MANUFACTURER B ONLY)

Four Manufacturer B parts failed during accelerated life due to an open internal wire bond at the post. Three parts contained an open bond at pin 1, one after 500 hours at 200°C, one after 4,000 hours at 225°C, and one after 250 hours at 250°C. One part contained an open bond on one of the pin 2 wires after 64 hours at 225°C. In each case, the three mil aluminum wire lifted from the gold-plated post. Separation occurred in the intermetallic zone, as shown in Figure F6-1 and F6-2, and the fracture surfaces were purple-colored. This indicated that the failure mechanism was Kirkendall 'oiding in AuAl₂. Because these failures were random, the excessive AuAl₂ was probably generated during the wire bonding operation.

6.2 OPEN PIN DUE TO BROKEN EXTERNAL LEAD

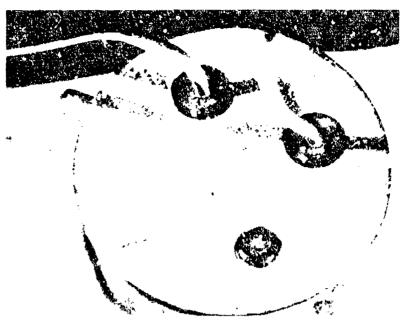
Three Manufacturer B and one Manufacturer D parts had to be removed from test because one of their external leads broke or fell off during insertion or removal from the lest socket. In the earliest (8 hour) Manufacturer B failure, the pin 1 lead broke at its point of egress from the glass insulator and most likely was mechanically overstressed by mishandling. In the other three instances, the pin 3 lead broke above the weld to the case. The Manufacturer D part broke cleanly with no sign of deterioration. Thus, the break probably was caused by mishandling or flexure of the leads during insertion and removal from the test socket. The welds of the two Manufacturer B parts were blackened, as illustrated in Figure F6-3. This condition was not present upon receipt of the parts and visual examination of life test survivors after 4,000 hours disclosed that the welds of almost every part had degraded to some degree. Usually the weld was blackened and there was a ring of discoloration in the gold plating of the header around the weld. Apparently, the weld of the Manufacturer B part also contains tin based solder and the tin had scavenged or leached gold from the header and the joint at elevated temperature thereby weakening the welds.



200X S/N 174 (64 HRS @ 225 C) FIGURE FG-1. LIFT-OFF PATTERN OF THE PIN 2 WIRE ROND



200x S/N 243 (250 HRS @ 250°C) FIGURE 16-2. EXAMPLE OF THE LILT-OFF PATTERN OF A PIN 1 WIRE BOND



S/N 264 (128 HR\$ @ 250°C)

FIGURE F6-3. EXAMPLE OF A PIN 3 LEAD FAILURE WITH
A BLACKENED WELD

6.3 AISCD FAILURES

Eight Manufacturer D parts and one Manufacturer B part failed during accelerated life due to excessive standby current drain change with load change ($\Delta I_{SCD}[13]$). $\Delta I_{SCD}[13]$ is the difference between the drain current at $I_L=-5$ mA ($I_{SCD}[9]$) and the drain current at $I_L=-500$ mA ($I_{SCD}[11]$). $\Delta I_{SCD}[13]$ has a specified minimum limit of -0.5 mA. The failed values ranged from -0.501mA to -0.640 mA. Bench tests of the parts confirmed the failed values, but examination of the test data disclosed that the $\Delta I_{SCD}[13]$ of these parts was probably out of tolerance or marginal upon receipt and this was not detected during the pre-life tests due to a list set malfunction. As shown in Table F6-1, $\Delta I_{SCD}[13]$ of the Manufacturer D parts was in tolerance and near zero (in some cases) initially and then out of tolerance or marginal at the next test point (4 hours into life). Two of the parts were left on test after failing and, through 4,000 hours, $\Delta I_{SCD}[13]$ did not vary more than two percent from the 4 hour value.

Examination of the control sample data ravealed the same pattern. As shown in Table F6-2, the $\Delta I_{SCD}[13]$ of the four control samples was near zero during the initial test and then significantly higher during every subsequent test. One part was marginal or out of tolerance during every subsequent test. Consequently, it is suspected that the 500 mA test current was not being applied to the part during the initial $I_{SCD}[11]$ measurement, due to a test set malfunction, and this caused the $\Delta I_{SCD}[13]$ values to be near zero or too low initially. The problem is suspected to be a stuck relay contact in the test set which corrected itself, since normal $\Delta I_{SCD}[13]$ values were obtained during the life tests. As indicated by the four hour values, $\Delta I_{SCD}[13]$ of these eight parts probably was out of tolerance or marginal upon receipt, consequently, these failures were not valid accelerated life failures.

TABLE F6-1. PARAMETER HISTORY OF THE \$1 SCD[13] FAILURES

Alsco	[;3]	•	mА
-------	------	---	----

CCLL	S/N	INITIAL	AT 4 HOURS	AT TIME OF FAILURE	AT 4,000 HE IKS
200°C	46	-0.000	0.540	(See 4 hours)	N/A
	145	-0.131	-0.640	(See 4 hours)	N/A
	143	-0.100	-0.500	<u>-0.530</u> (64 hours)	H/A
225°C	164	-0.070	-0.430	-0.520 (16 hours)	k/A
250°C	264	-0.050	-0.530	(See 4 hours)	-0.540
	? 82	~0.111	-0.520	(See 4 hours)	N/A
	233	-0.120	-0.500	-0.560 (16 hours)	M/A
	271	-0.060	-0.500	-0.500 (1000 hrs)	-0.490

NOTE: FAILED VALUES ARE UNDERLINED.

TABLE F6-2. ΔI_{SCD} [13] HISTORY OF THE CONTROL SAMPLES

Δ1_{SCO}[13] - mA

<u>S/N</u>	4/8/77 (INITIAL)	8/1/77 (4 HOUR I)	8/8/77 (4 HOUR [1]	4/22/78 (4,000 HRS)
11	-0.010	-0.500	-0.500	-0.540
12	-0.111	-0.290	-0.290	-0.290
13	-0.030	- C.350	-0.350	-0.350
14	-0.010	-0.350	-0.340	-0.330
15	-0.000	-0.230	-0.230	-0.246

7.0 723 FAILURE ANALYSIS REPORT

7.1 i_{SCD} FAILURE (MANUFACTURER C ONLY)

Six Manufacturer C parts exhibited excessive standby current drain (I_{SCD}) after 2,000 hours at 200°C. I_{SCD} has a specified maximum limit of 3.0 mA and the failed values ranged from 3.001 to 3.066 mA. Three of the parts were returned to life test after failing, and all were within specification at 4,000 hours. All six parts were then returned to life test for an additional 2,000 hours, after which their I_{SCD} values were virtually the same as the pre-stress values. The I_{SCD} history of the parts is shown in Table F7-1. Examination of the control sample data, also given in Table F7-1, indicated that a current sensing resistor in the test set had drifted causing an average error of +0.153 mA in I_{SCD} of the control samples at the 2,000 hour test point. Adjusting the I_{SCD} values of the six 2,000 hour failures accordingly brings all of the values to within specification. Consequently, these failures were attributed to test set drift rather than any part deficiency.

7.2 -55°C FAILURES (MANUFACTURER C ONLY)

One Manufacturer C part failed V_{RLINE}[1] and V_{RLOAD}[4] at -55°C at 4,000 hours and one Manufacturer C part failed V_{REF} at -55°C at 4,000 hours. • The failures appeared to be catastrophic; therefore, the parts were retested at 25°C and were found to be within specification. The parts were returned to life for an additional 2,000 hours after which the failed parameters were within specification and virtually the same as the pre-life values, as shown in Table F7-2. Microscopic examination of the interior of the parts plus pull testing of the wire bonds disclosed no intermittencies which could account for the 4,000 hour failures. Therefore, these failures were probably caused by test socket intermittencies during the -55°C test at 4,000 hours.

7.3 J_{OS} FAILURES (MANUFACTURER D ONLY)

Two Manufacturer D parts failed I_{OS} during 175°C accelerated life. As shown in Table F7-3, one part was marginal upon receipt and simply drifted out of specification at the first test point (4 hours). Consequently, this

TABLE F7-1. ISCD HISTORY

J_{SCD} @ 25°C (mA) [SPEC = 3.0 mA MAX.]

CELL	<u> </u>	PRE-STRESS	1,000 HOURS	2,000 HOURS	4,000 HOURS	ADDITIONAL 2,000 HOURS
200°C	232	2.658	2.830	3.001	2.916	2.668
	235	2.641	2.839	3.035	2.927	2.672
	313	2.656	2.792	3.015	2.885	2.630
	34]	2.673	2.801	3.065	-	2.646
	363	2.626	2.760	3.024	-	2.603
	371	2.662	2.796	3.058	-	2.637
CONTRO	LII	2.105	2.240	2.231	2.322	2.087
	12	1.643	1.758	1.792	1.816	1.630
	13	2.059	2.184	2.223	2.262	2.043
	14	1.863	1.975	2.013	2.048	1.849
	15	1.539	1.634	1.665	1.699	1.532
	NEAN	1.842	1.953	1.995	2.029	1.828
	MEAN A t-t _{pre-s}	TRESS)	+0.116	+0.153	+0.187	-0.014

TABLE F7-2. PARAMETER HISTORY OF THE -55°C FAILURES

			CDECLETE			
<u>CELL</u>	<u>S/N</u>	PARAMETER	INITIAL	4,000 HOURS	6,000 HOURS	SPECIFIED LIMIT
200°C	325	v _{RLINE} [1] (%)	-0.016	-162.878	-0.012	3 to .3
		V _{RLOAU} [4] (2)	-0.018	+1.704	-0.016	6 to +.6
	334	V _{REF} (VDC)	7.075	0.000	7.076	6.90-7.40

NOTES

1. FAILED VALUES ARE UNDERLINED.

TABLE F7-3. PARAMETER HISTORY OF THE I_{OS} FAILURES $I_{OS} \text{ (mA) (SPECIFIED LIMIT = 45 - 85 mA)}$

CELL	<u>s/n</u>	INITIAL	4 HOUR	32 HOUR	64 HOUR	BENCH TEST
175°C	175	83.3	86.1	-	-	-
	162	50.6	56.1	56.2	86.0	64.0
REF: CONTROL	(MEAN OF	62.4	63.4	62.0	61.2	•

NOTES

1. FAILED VALUES ARE UNDERLINED.

failure was not investigated further. The other part failed marginally and was back within specification when bench tested. This indicated that the failure mechanism was probably surface related and no further investigation was performed on this single isolated failure.

8.0 LM111 FAILURE ANALYSIS REPORT

8.1 V_{10} FAILURE DUE TO DEGRADED Q4

Buring step-stress and life test, 93 Manufacturer D parts and 6 Manufacturer B parts failed due to excessive $\rm V_{IO}$. These parts failed combinations of the first four specified $\rm V_{IO}$ parametric tests and the failed values ranged from +5.01 mV to +11.02 mV. The parts would recover when baked which indicated that the failures were caused by a surface instability mechanism.

Analysis of these parts established that the excessive V_{IO} was caused by a gain mismatch in the NPN input transistors, Q3 and Q4. In each part examined, h_{FE} of Q4 was lower than that of Q3 as illustrated in Table F8-1. When baked (100 hours at 250°C), h_{FE} of Q4 improved two to three-fold as also illustrated in Table F8-1. The bake also caused a slight decrease in h_{FE} of Q3 but this is apparently due to a separate annealing effect since h_{FE} of both transistors of a unstressed control part decreased when baked as shown in Table F8-1.

The reversible gain decrease displayed by Q4 indicates that the degradation probably was caused by depletion or inversion of the p-type base region due to the accumulation of a net positive charge in or on the passivation over the base. The collector-base junction of Q4 was reverse biased during life test, consequently the accumulation was the result of charge separation in the fringing field of the reverse biased junction.

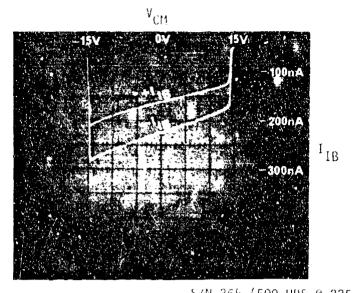
TABLE F8-1 - EXAMPLE OF THE RESULTS FROM DIE LEVEL PROBING OF REPRESENTATIVE VIO

					h _{FE} @ I _C = 29	mA, V _{CE} = 15V
MANUF	CELL TEMP	S/N	TIME OF FAILURE	TRANSISTOR	^{0t} F	POST BAKE
Đ	250°C	62	1,000 HRS	Q3 Q4	210 43	180 104
D	200°C	135	1,000 HRS	Q3 Q4	174 32	145 101
D	CONTROL (REFERENCE	15 E)	(UNSTRESSED)	Q3 Q4	207 235	174 154

8.2 I_{10} FAILURE DUE TO SURFACE AND BULK MECHANISMS

During step-stress and life test, 64 Manufacturer B parts and 5 Manufacturer D parts failed due to excessive I_{10} . Of these 69 parts, 61 failed I_{10} [11]. Seven parts failed I_{10} [9] and one part failed I_{10} [8]. I_{10} [11] is the raised input offset current, I_{10} (R), which is the difference of the input bias currents, $-I_{1B}$ (R) and $+I_{1B}$ (R), measured at $+V = \pm 15V$ and $V_{CM} = 0V$ and with BAL/STB and BAL connected to +V. I_{10} (R) has specified limits of -25 nA MIN and +25 nA MAX. In 56 parts I_{10} (R) was positive, because the inverting input bias current, $-I_{1B}$ (R), was greater than the noninverting input bias current, $+I_{1B}$ (R), as illustrated in Figure F8-1. The failed values ranged from +25 nA to +151 nA. In five parts I_{10} (R) was negative, because $+I_{1B}$ (R) was greater than $-I_{1B}$ (R), and the failed values ranged from -26 nA to -30 nA.

Analysis of parts with positive excessive $I_{IO(R)}$ established that the failures were caused by a gain mismatch in the PNP input transistors. The input bias currents are the base currents of the PNP input transistors QI and Q2. $+I_{\ \ IB}$ is the quotient of $h_{\ \ FE}$ of Q1, the noninverting input transistor, and I_C of Q1 (+ $I_{IB} = I_{C1}/h_{FE}$). Likewise, - I_{IB} is the quotient of h_{FE} of Q2, the inverting input transistor, and I_C of Q2 (- $I_{IB} = I_{C2}$ / $\mathbf{h}_{\mathrm{FF}})$. Die level probing of representative failures established that the collector currents of Q1 and Q2 were equal, but that $h_{\rm FF}$ of Q2 was lower than h_{FE} of Q1, as shown in Table F8-2, which is why $-I_{IB(R)}$ was greater than $+I_{IB(R)}$. To determine what change took place during life test, the test data was examined. $+I_{IB(R)}$ and $-I_{IB(R)}$ were not measured during the tests (they are not specified parameters), but $+I_{IB}[12]$ and $-I_{IB}[12]$ were measured. $+I_{IR}[12]$ and $-I_{IR}[12]$ are the input bias currents at $\pm V = \pm 15V$ and $V_{CM} = 0$ volts with BAL and BAL/STB open (dc wise). As shown in Table F8-3, the values of $+I_{IB}[12]$ and $-I_{IB}[12]$ of the representative failure before and after accelerated life indicate that the gain of both transistors decreased during life, but that $h_{\rm FE}$ OF Q2 decreased more than did $h_{\rm FE}$ of Q1.



S/N 265 (500 HRS @ 225°C) FIGURE F8-1 - $+1_{\mathrm{IB}}$ AND -1_{IB} (RAISED) VS. COMMOG MODE VOLTAGE OF A PART WITH LXCLSSIVE 1 IU(R)

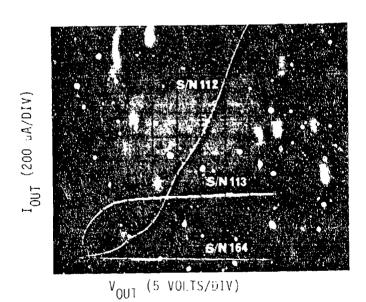


FIGURE F8-2 - I-V CHARACTERISTIC FROM OUTPUT (+ ON PIN 7) TO SUBSTRATE (- ON PIN 4)

OF THE THREE PARTS WHICH HAD TAILED 10

TABLE F8-2 - RESULTS OF DIE LEVEL PROBING OF OI AND 02 OF REPRESENTATIVE IO(R) FAILURES

92 hFE/91 hFE	.73	.71	*74	1.00	.75
10(R)* -118(R)* +118(R)* hFE @ 1C = 20M & VCE = 5V +118(R)/-118(R) Q2 hFE/Q1 hFE	69.	.68	74	26 ,	64.
JuA & V _{CE} = 5V -	182	168	213	260	278
hFE @ 1c = 20	250	238	286	260	370
+1 _{18(R)} *	-180 nA	-210 rA	-185 rA	-130 r.A	-150 mA
IB(R)*	+80 nA -260 nA -180 nA	+100 nA -310 nA -210 rA	+65 nA -250 nA -185 rA	+12 nA -192 nA -180 nA	+40 nA -190 nA -150 mA
10(R)	+80 nA	+100 nA	+65 nA	+12 nÅ	+40 nA
TIME OF REMOVAL	1,000 HR	1,000 HR	1,000 HR	ı	500 HR
TIME OF	1,000 HR		500 HB		500 HR
S/N/S	155	211	52	231	42
CELL	200°C 155	255°C	ວ≥057	UNSTRESSED 231	250°C 42
MANUF	æ	. ca	œ	æ	۵

*CURVE FRACER TEST DATA AT TIME OF REMOVAL

TABLE F8-3 - +I IB (VCM = OV) HISTORY OF THE REPRESENTATIVE I IO(R) FAILURES

			PARAME T	ER VALUES (NA)
MANUF	S/N	PARAMETERS	INITIAL	TIME OF REMOVAL
В	155	+1 ₁₈ [12]	-59	-67
		-1 ₁₈ [12]	-60	-75
В	211	+1 ₁₈ [12]	-71	-7 7
		-1 _{IB} [12]	-73	-96
В	52	+I _{IB} [12]	-63	- 73
		-1 ¹⁸ [15]	-65	-80
D	42	+118[12]	~38	-41
		-1 ₁₈ [12]	-38	-45

Sample failed parts were baked (some after delidding and removing the glassivation) for about 80 hours at the test cell temperature. In each part, I_{100RM} recovered as shown in Table F9-4. In the 200°C failures, $I_{1B(R)}$ decreased after baking which indicated that $h_{\rm FF}$ of Q2 improved (increased) upon baking. However, in the 225°C and 250°C failures, $-I_{IR(R)}$ and $+I_{IB(R)}$ usually increased after baking which indicated that $h_{\rm FF}$ of Ql and Q2 further decreased upon baking. The decrease in $h_{\rm FE}$ of Q1 was greater than that of Q2; consequently, $I_{10(R)}$ was within specification after baking. These findings indicated that the ${\rm I}_{10}$ failures were caused by two degradation mechanisms, a surface related (reversible) mechanism predominant at 200°C and a bulk related (nonreversible) mechanism which predominated at the higher temperatures. The surface related mechanism probably was similar to that responsible for the V_{ID} type failures described in Section 8.1. The cause of the bulk mechanism was not established. Electrical evaluations of the p-n junctions of degraded transistors disclosed no abnormal characteristics and optical examinations of the transistors disclosed no visible anomaly which could account for the gain degradation.

8.3 I_{1B} FAILURE DUE TO AMPLIFIER SATURATION (MANUFACTURER B ONLY)

During step-stress two parts failed due to excessive $\pm I_{1B}[13]$. In each case $\pm I_{1B}[13]$ was positive (± 32 nA and ± 107 nA); normally $\pm I_{1B}$ is negative. $\pm I_{1B}[13]$ is the noninverting input bias current at a common mode voltage of ± 14.5 V and supply voltages of ± 15 V. Examination of the input bias currents of these parts on the curve tracer disclosed that as the common mode voltage approached the specified values of ± 14.5 V and ± 13 V, ± 11 B decreased sharply toward positive values due to saturation of the amplifier. This effect is illustrated in Figure 13 of the main report. Repeated retests of the two failed parts and other sample parts on the test set disclosed that all parts would intermittently pass and fail ± 11 B. This indicated that the device could not operate consistently at the specified common mode voltages; i.e., the specified common mode voltages were too close to the supply voltages. Consequently, the common mode voltages were reduced to ± 13.5 V and ± 12 V. Subsequent to this change no further ± 11 B failures of this type were encountered during step-stress and accelerated life.

TABLE F8-4 - RESULTS OF BAKE OF REPRESENTATIVE I 10(R) FAILURES

CEI L TEMP	S/N	TIME OF FAILURE	PARAMETER	VALUE PRIOR TO BAKE (nA)	VALUE AFTER BAFE (nA)	DIRECTION OF CHANGE IN h _{FE} of Q1 or Q2
250°C	114	1,000 HRS	+1 _{1B(R)}	-220	-300	DECREASE
			-1 _{18(R)}	-246	-285	DECREASE
			(9)01	26	-15	
	102	1,000 HR\$	+1 _{1B(R)}	-240	-242	MONE
			-1 _{18(R)}	-267	-23 5	INCREASE
			1 _{19(R)}	47	7	
	84	500 HRS	†138(R)	-149	-176	DECREASE
			-1 _{1B(R)}	-183	-193	DECREASE
			1 _{10(R)}	34	17	
	92*	4 HRS	+1 _{18(R)}	-161	-218	DECREASE
			-1 _{18(R)}	-197	-218	DECREAGE
			I _{10(E)}	26	0	
2 25° C	242	1,000 HRS	+1 _{18(R)}	-136	~20C	DECREASE
			-1 _{IB(R)}	-176	-200	DECREASE
			1 _{10(R)}	40	9	
	223	1,000 HRS	+1 IB(R)	-128	-205	DECREASE
			-I _{IB(R)}	-160	-205	DECREASE
			1 _{10(R)}	52	0	
	192	64 HRS	+1 _{1B(R)}	-128	-200	DECREASE
			-1 _{18(P)}	-168	-210	DECREASE
			110(p)	40	10	
200'Ç	142	1,000 HRS	+I;B(R)	-188	-174	INCREASE
			-1 _{18(R)}	-220	-166	INCREASE
			I;O(R)	3 2	12	
	144*	1,000 HR	+1 B(R)	-192	-190	NONE
			-1 _{18(R)}	-222	-192	INCREASE
			110(R)	30	2	
	143	500 HRS	+1 _{18(R)}	-222	-274	MONE
			·I/B(R)	-257	-226	INCREASE
			1 _{10(P)}	30	2	

NOTES:

1. ALL PARTS WERE MAJED AT THE CELL TEMPERATURE FOR 80 HORAS.

2. PARAMETER VALUES MERE MEASURET, ON A 577 CURVE TRACER.

8.4 10 FAILURE DUE TO DEGRADED Q15 (MANUFACTURER 8 ONLY)

During accelerated life, three Manufacturer B points failed due to excessive $I_0[16]$ which is the output leakage current with 32V applied to the collector of Q15. The failed values ranged from 0.589 to 60.1 microamperes. Examination of the parts on the curve tracer disclosed a channeled characteristic between pin 7 (output) and pin 4 (-V) in one device, a quasi-exponential characteristic in one device, and no leakage in one device (I_0 had recovered) as shown in Figure F8-2. The leakage was traced to the collector-to-substrate diode (isolation junction) of the NPN output transistor Q15. The leakage dropped to zero when the parts were baked indicating that the degradation was caused by a surface related mechanism, probably inversion of the n-type collector tub of Q15. During life test the collector-substrate junction of Q15 was reverse biased (the output was high); consequently, the inversion probably was the result of charge separation in the fringing field of the reverse biased junction.

9.0 REFERENCES

- [1] J. M. Patterson, "A Technique to Locate Leakage Current on Semiconductor Devices," Proceedings of Advanced Techniques in Failure Analysis,
 September 1977, pages 90-93.
- [2] J. R. Haberer and J. J. Bart, "Charge Induced Instabilities in 709 Operational Amplifiers," 10th Annual Proceedings, Reliability Physics 1972, pages 106-111.

APPENDIX G
INITIAL JAN QUALIFIED DEVICE FAILURES

APPENDIX G JAN QUALIFIED DEVICE FAILURES

Upon receipt at MDAC-St. Louis, all devices were subjected to external visual examinations, hermeticity test, and electrical test. During these tests, five of Manufacturer D's MIL-M-38510/10201 JAN qualified devices were found to be defective. Two devices were rejected during the visual inspection test. Shown in Figure G1 is a device which has been physically damaged and in Figure G2 a device is shown with a cavity in the package base. During the fine leak hermeticity tests one device failed with a leak rate of 2.0×10^{-6} atm cc/sec. Initial data taken at 25° C, $+125^{\circ}$ C and -55° C is shown in Figure G3 for the two devices (S/N 301 and S/N 302) which did not meet the electrical specifications. No further data was taken on any of the five failed devices.



FIGURE GT. DAMAGED M38510/10201



FIGURE G2. CAVITY IN BASE OF M38510/10201

CELL TENP 25 C	15.57th 0.71 25.C. 14.04bit.) 14.04b	#38010710201	TEST TIME O HAS		
15-37E 0 AT 25 C. WHUMBOR AT 25 C. WHUMBOR AT X X VIDC HANDC -0 316* 0 0000 0 005 7 132 56 719 7 -0 316* 0 0000 0 005 7 242 5719 7 TEST TIPE: 0 HRS CELL TEHP: 25 C. TESTED AT: 125 C. WHUMBOR AT: 125 C. WHOW AT: 125 C. WHUMBOR AT: 125 C. WHUMBOR AT: 125 C. WHUMBOR AT: 125 C. WHOW AT: 125 C. W	15-3FED AT 25 C.				
VHLUADID(A) VKLGADI(S) VYLGADI(S) VYLGAD	VPLOADIG (4) VPLOADIG (5)				
7. 7. 7. 7. 10000 HVIDC HVIDC 1.0 316** 0 000 0 0 005 7 132 55 7126 TEST TIME: 0 MES CELL TEMP. 25 C TESTED AT: 125 C VHLOADIG (4) VRLOADIG (5) VRLOADIG (6) VREF 7. 242 55 7126 TESTED AT: 125 C VRLOADIG (5) VRLOADIG (6) VREF 7. 25 C VRLOADIG (6) VRLOADIG (7) VREF 7. 154 0.000M 9. 0000M 7. 154 0.000M	TESTED AT TESTED AT TESTED AT	WEING (Z) VREINE (3)	VHLGAB(A) VRLGAB(S)	108	15.0
-0 316* 0 000 7 7 132 56 719 TEST TIME: 0 MPS CELL TEMP. 25 C TESTED AT: 125 C VMLOAD(4) VRLOAD(5) VRLOAD(6) VRCF 105 -0 380 0 000M 0 000M 7.154 0.000M -0 340 0 000M 0.000M 7.154 0.000M	10 3164 0 000 0 005 7,242 5,6 719 TEST TIPE 0 PRS	×	**	MADC	MODE
TEST TIME: 0 MPS CELL TEMP. 25 C TESTED AT: 125 C VHLGAD(4) VRLGAD(5) VRLGAD(6) VRCF 105 A X X VDC MADC -0 330 0 000M 0 000M 7, 154 0, 000M -0 343 0 000M 0, 000M 7, 279 0, 000M	TEST TIME: 0 MRS CELL TEMP: 25 C TESTED AT: 125 C VMLOAD(4) VMLOAD(5) VMLOAD(6) VMRCF 105 N	20 104 60 10 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	-0 316* 0 000 -0 246* -0 003	58 719 57 126	2 660 2 453
TEST TIME: 0 HPS CELL TEMP. 25 C TESTED AT: 125 C VMLOADI(4) VRLOADI(5) VRLOADI(6) VREF 105 \(\lambda \) \(\times \)	TEST TIME: 0 HPS CELL YEMP. 25 C TESTED AT: 125 C VMLGAD(5) VRLGAD(6) VREF 105 N				
CELL TEMP. 25 C TESTED AT: 125 C VALOAD(4) VALOAD(5) VALOAD(6) VREF IOS A X X VDC MADC -0 380 0 000M 0 000M 7.154 0.000M -0 343 0 000M 0.000M 7.279 0.000M	TESTED AT: 125 C	16VICF 17/N M36510/10201			
TESTED AT: 125 C VALOAB(4) VALOAB(5) VALOAB(6) VAREF 10S 2	TESTED AT: 125 C				
VALIDADI(4) VALIDADI(5) VALIDADI(5) VALIDADI(6) VREF TOS -0 330 0 000M 0 000M 0 000M 7, 154 0, 000M -0 343 0 000M 0 000M 7, 279 0, 000M	VRLGAB(4) VRLGAB(5) VRLGAB(6) VRREF 10S N x x vbc MADC N 0.343 0.000M 0.000M 7.154 0.000M N 0.343 0.000M 7.279 0.000M TEST FIME 0.465 0.000M 7.279 0.000M CELL IFMO 25 C. 105 105 TESTED AT -55 C. 2 105 NRLSAB(A) VRLSAB(B) VRLSAB(B) VRLSAB(B) N -0.273 0.000M 7.104 PHDC N -0.126 0.000M 7.104 0.000M				
-0 350 0 000M 0 000M 7, 154 0, 000N -0 343 0 000M 0, 000M 7, 279 0, 000N	1-0.343 0.000N 0.000N 7.154 0.000N 0.000N 7.279 0.000N 0.000N 7.279 0.000N 0.000N 7.279 0.000N 0.000N 7.279 0.000N 0.000N 7.279 0.000N 0.000N 7.279 0.000N 0.000N 0.000N 7.279 0.000N 0.000N 0.000N 7.203 0.000N 0.0	VR. INE(2) VR. INE(3)	VRLGAD (5)	108	ISCD
-0.380 0.000N 0.000N 7.154 0.000N -0.343 0.000N 0.000N 7.279 0.000N	-0.340 0.000M 0.000M 7.154 0.000M TEST TIME 0.46S. CELL TFMP. 25 C. TESTED AT -55 C VRLGADI 4) VRLGADI 5) VRLGADI 6) VREF 105 7	*	ж	MADC	MADC
	TEST TIME: 0 HRS. CELL TEMP: 25 C. TESTED AT -55 C. VRLGCD1A) VRLGAD(5) VRLGAD(5) VREF 105 A X X UDC HHDC -0.273 6 000M 0 000M 7, 106 0 000M -0.186 0 000M 0 000M 7, 201 C, 000M	NC00 0 NC00 0	-0 380 0 000N	0, 0000N	2.035 1.810
	25 C. -55 C. -75 C. -78 C.	JAVIGE PAN, MBSS1C/10201			
	-55 C VRL 0AD (5) VRLOAD (6) VREF 10S X X VINC IMUD: 6 000M 0 000M 7, 106 0 000M 0 000M 0 000M 7, 201 C, 000M				
74	VRLScB(4) VRL OAD (5) VRLCAND (6) VREF 105 2 X X VINC MHDC -0.273 0.000M 0.000M 7.104 0.000M -0.186 0.000M 0.000M 7.201 0.000M				
4 h	X X VIIC MHIDT 6 000N 0 000N 7.106 0 000N 0 000N 7.201 0.000N	VRL INE (2) VRL INE (3)	VRL 0A0 (S)	105	1SCD
0 HRS. 25 C55 C75 C78	-0.273 6.000N 0.000N 7.106 0.000N -0.186 0.000N	×	ж) de ¥	₹ 50
25 C55 C55 C74 VRLOAD(5) VREF 105		H000 0 NCC0 0	**************************************	N000 0	3, 326

FIGURE 93. INITIAL ELECTRICAL DATA FOR MANUFACTURER D'S M38510/10201 FAILED DEVICES

MANUFACTURER CODE

MANUFACTURER	CODE
Precision Monolithics Inc.	А
National Semiconductor Corp.	В
Advanced Micro Devices	С
Fairchild Semiconductor Corp.	D

nus Government Printing Office: 1979-614-023/207

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